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RADIATION CHARACTERIZATION OF SEQUENTIAL LOGIC CIRCUITS.(U)
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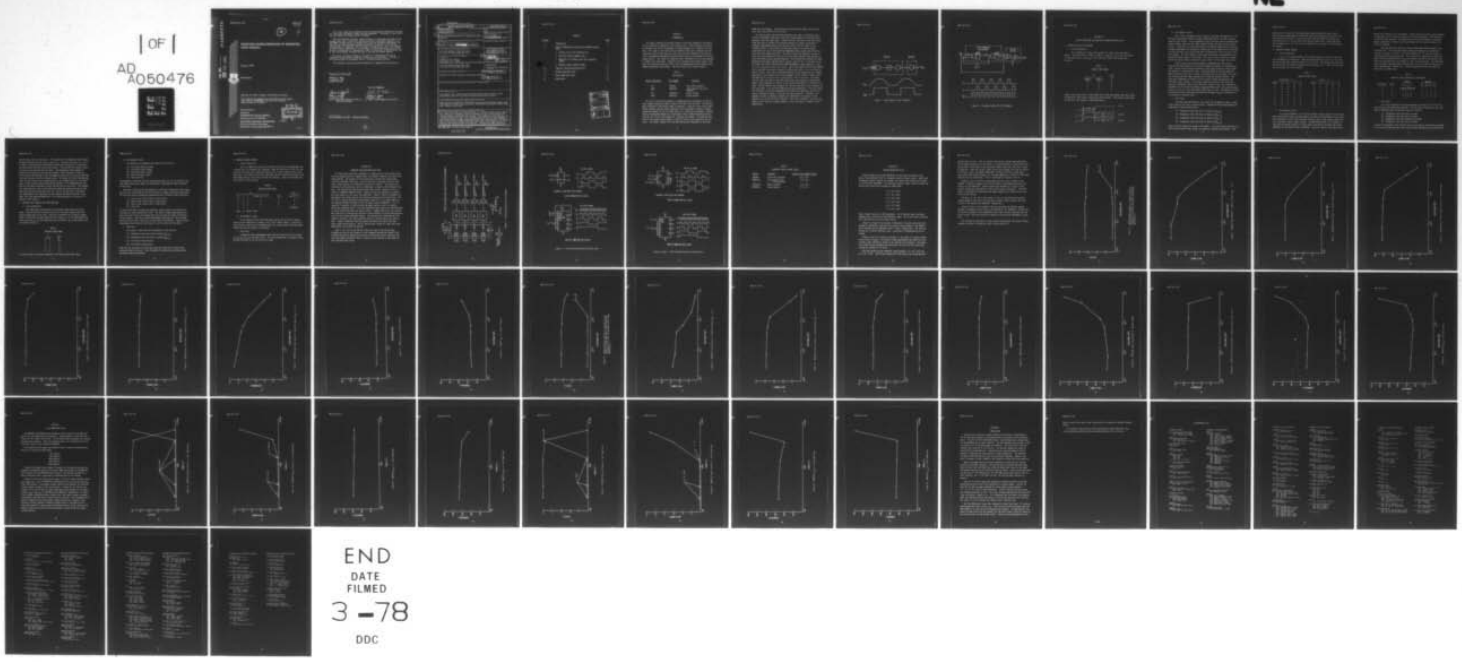

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RADIATION CHARACTERIZATION OF SEQUENTIAL LOGIC CIRCUITS

January 1978

Final Report

Approved for public release; distribution unlimited.

This research was sponsored by the Defense Nuclear Agency under Subtask Z99QAXTB029, Work Unit 62, Radiation Characterization of MSI/LSI.

Prepared for
Director
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Washington, DC 20305

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes the test techniques for radiation characterizing medium and large-scale integration (MSI/LSI) sequential logic circuits where few internal nodes are available for testing. Four sequential logic devices, two transistor-transistor-logic (TTL) technology devices and two complementary-metal-oxide-silicon (CMOS) technology devices were characterized. The devices were characterized for gamma dose-rate logic upset, total gamma dose survivability, and neutron fluence survivability. The data has been analyzed to determine the applicability of the testing techniques and procedures.

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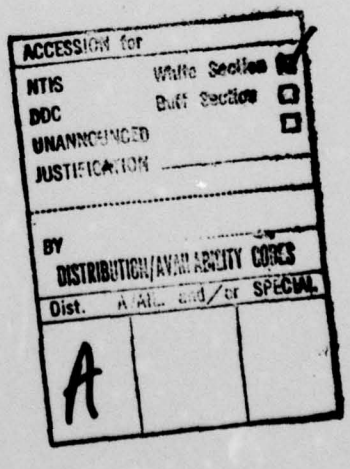
CONTENTS



SECTION I

INTRODUCTION

This report examines the various types of electrical parametric tests which can be conducted on sequential logic circuits (e.g., shift registers, counters) to determine the circuit performance following exposure to a radiation environment. The intent of this effort was to identify those test techniques and test conditions which provide the most useful and accurate information in analyzing circuit performance degradation resulting from transient and permanent radiation damage effects. Four types of sequential logic integrated circuits were employed to conduct this experiment. Eight-bit shift registers and binary counters from both the transistor-transistor-logic (TTL) and complementary metal-oxide-silicon (CMOS) technologies were tested. The four circuits are listed in table 1.

Table 1

TEST DEVICES

Device Technology	Part Number	Function
TTL	SN7491A	8-bit shift register
CMOS	MM74C164	8-bit parallel out shift register
TTL	SN74LS197	binary counter
CMOS	MM74C163	binary counter

All four circuits were exposed to a gamma dose-rate environment in the Air Force Weapons Laboratory (AFWL) Febetron 705 flash X-ray facility. The circuits were irradiated in the dynamic mode of operation. Since all four circuits were tested through transient upset conditions, this experiment provided a hardness comparison between the TTL and CMOS devices in a dose-rate environment. Because neutron displacement damage has a negligible effect on MOS technology devices, only the TTL circuits were exposed to a neutron environment. The exposure took place at the Sandia Pulsed Reactor II (SPR II) with no bias applied to the circuits. For similar reasons, only the MOS devices were subjected to the total

gamma dose environment. This was done at the AFWL Co-60 gamma source with a worst case bias applied to the circuits.

All circuits were characterized both before and after irradiation using a Fairchild 5000/5800 integrated circuit test system capable of performing only parametric and time delay tests. Control devices from each of the four device types were used to monitor the Fairchild system for internal variations in parameter measurement which could adversely affect the data taken on the irradiated parts. Two external circuits were required to provide signal conditioning for two of the Fairchild 5000/5800 output signals which interface with the device under test (DUT). The first circuit was needed to correct a pulse rise time problem--for the TTL circuits--which resulted from the need to clock the devices during characterization. The clocking was performed by reprogramming the DC power supplies from a logical input "0" to "1" and back to "0." The pulse rise time of the Fairchild 5000 programmable power supplies is about 15 μs for transitions from 0 to 3 volts. Due to the speed at which they operate, the TTL devices could easily mistake a single pulse with a 15 μs rise time for several pulses. The slower running MOS devices did not experience this anomaly. Therefore, a pulse shaper circuit was designed, using a Schmitt trigger, which provided the TTL circuits with a pulse having a 10 ns rise time. The second circuit, which was used for the time delay tests, was required to produce the proper clock frequency for the DUT using the pulse generators in the Fairchild 5800. The DUT requires one frequency for the data and double that frequency for the clock pulse. The Fairchild 5800 has two pulse generators. The pulse width and time delay can be set independently for each pulse generator; but the frequency, although variable, is the same for both generators. Therefore, the external circuit--a frequency doubler--was connected to the output of one generator to provide the clock frequency. The circuit schematics for the pulse shaper circuit and the frequency doubler circuit are shown in figures 1 and 2, respectively.

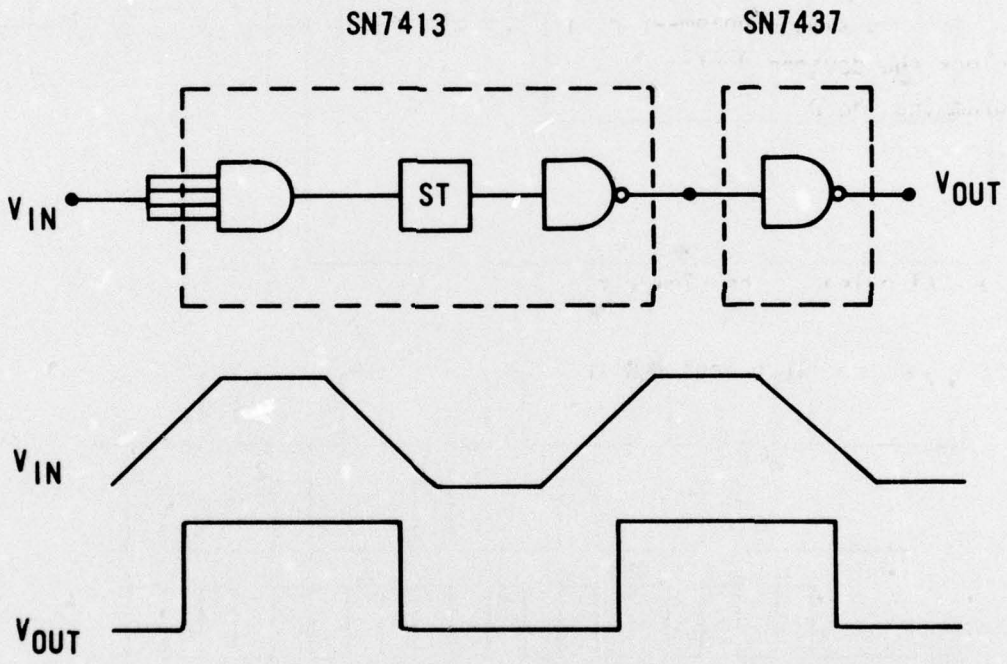


Figure 1. Pulse Shaper Circuit Schematic

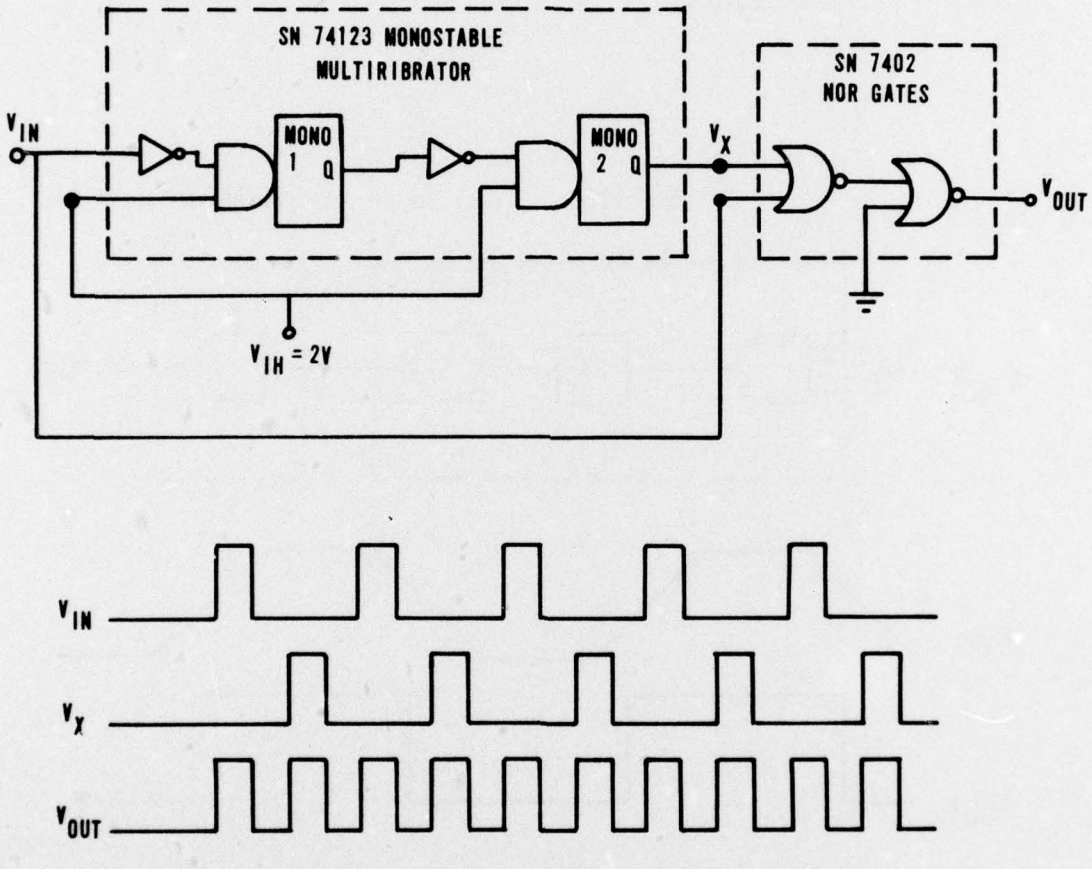


Figure 2. Frequency Doubler Circuit Schematic

SECTION II

CIRCUIT OPERATION AND ELECTRICAL CHARACTERIZATION TESTS

1. SN7491A 8-BIT SHIFT REGISTER

a. Circuit Operation

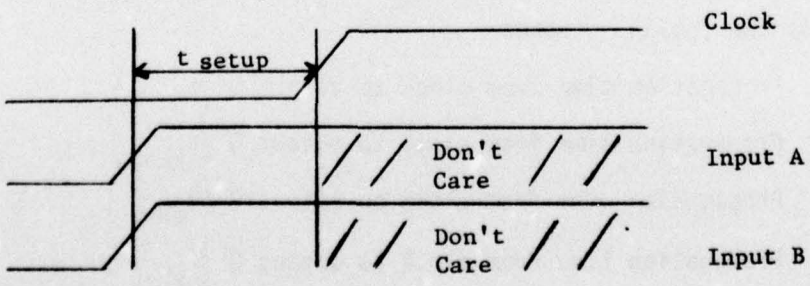
This standard TTL 8-bit shift register is serial input and serial output. The truth table is shown in table 2. Note that t_n is the time before a clock pulse occurs, and t_{n+8} is the time after eight clock pulses have occurred.

Table 2

SN7491A TRUTH TABLE

t_n		t_{n+8}
Input A	Input B	Q
0	0	0
0	1	0
1	0	0
1	1	1

Inputs A and B must be in a logic state for a given time before the clock occurs to enable the logic state to enter the shift register. This time is called the set-up time. The timing is illustrated below.



b. DC Parametric Tests

All of the dc parametric tests listed in the Texas Instruments (TI) TTL Data Book specification sheet, and some additional special dc tests, were performed on this device. The dc parametric tests listed by Texas Instruments were output voltage, input current, power supply current, and short circuit output current. Since this is a two-input device, the correct output state for output voltage measurements was obtained by holding one of the inputs at 2.5 volts and clocking the other input eight times with the appropriate input high and input low voltages. The test system is restrained from making any measurements until determined states appear at the output. The special tests consisted of determining the output current required to cause a shift in the output logic level.

These special tests were performed to determine the sink current required to cause outputs Q and $\overline{Q}$ to shift above the logical "0" specification level, and the source current required to cause output Q and $\overline{Q}$ to shift below the logical "1" specification level. Since the amount of current which the output transistor can sink or source is directly tied to the fanout, this test will indicate how the fanout changes with increasing radiation levels. The tests were conducted by forcing a sink or source current and measuring the resultant output voltage. The current, which was initially less than that required to produce a zero or one state for a fanout of ten, was increased in increments of 0.5 ma and the output voltage monitored until a one state dropped below 2.4 volts or a zero state went higher than 0.4 volt. The amount of current at which the failure occurred determined the allowable fanout of the device at the particular radiation level.

c. Time Tests

The time tests performed on this device were propagation delay, output pulse rise and fall time, and set-up time. Propagation delay measurements were conducted for the following cases:

(1) Propagation time from clock to output Q $\left(t_{pL-H}\right)$

(2) Propagation time from clock to output $\overline{Q}$ $\left(t_{pL-H}\right)$

(3) Propagation time from clock to output Q $\left(t_{pH-L}\right)$

(4) Propagation time from clock to output $\overline{Q}$ $\left(t_{pH-L}\right)$

Each of the four cases was tested in two modes. First one input was held at 2.4 volts and the second input pulsed, and then the situation was reversed. The

output pulse rise and fall time measurements were performed on both Q and $\overline{Q}$. This was also accomplished by holding one input high and pulsing the other, and then reversing the inputs. Set-up time tests were performed by delaying the clock pulse by 0, 5, 12, 24, and 30 ns from the input pulse. These time tests are performed with a TTL load--which is equivalent to a fanout of 10--applied to the outputs.

2. SN74LS197 BINARY COUNTER

a. Circuit Operation

This is a low power Schottky TTL four-bit counter in which all the bits are programmable or presettable. When the count/load input is set low, the bits are set to the logic states on inputs A, B, C, and D. The counter can also clear the bits to the "0" state by setting the clear input to "0." Table 3 illustrates the truth table for clock counting.

Table 3

SN74LS197 TRUTH TABLE

Count/Load = "1"					Clear = "1"				
Count	Q_D	Q_C	Q_B	Q_A	Count	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0	8	1	0	0	0
1	0	0	0	1	9	1	0	0	1
2	0	0	1	0	10	1	0	1	0
3	0	0	1	1	11	1	0	1	1
4	0	1	0	0	12	1	1	0	0
5	0	1	0	1	13	1	1	0	1
6	0	1	1	0	14	1	1	1	0
7	0	1	1	1	15	1	1	1	1

b. DC Parametric Tests

As with the SN7491A, all of the dc parametric tests listed in the TI Data Book specification sheet, and some special dc tests, were performed on this device. The dc parametric tests included output voltage, input current, power supply current, and short circuit output current. The additional tests, sink current in a low state and source current in a high state, were used to determine the fanout capability of the device after irradiation. The first special test required the

device to be cleared to all low levels. A sink current was forced, and increased in magnitude, until an output voltage of 0.5 volt was achieved. The resulting current was then recorded. The second special test was performed in the same manner, except that a source current was forced until an output voltage of 2.7 volts was obtained.

The high-level and low-level output voltages were both obtained in two different ways. The high-level output voltage was obtained by clocking the counter to a count of 15 (all "1"s) and by loading all "1"s from the input to the output with the count/load low. The low level was obtained by setting the clear low (which automatically drives all outputs low) and by setting the clear high, the count/load low, and loading all "0"s into the counter. The high-level output voltage is measured while sourcing 800 μA, and the low-level output voltage is measured whil sinking 8 mA. Table 4 presents the output voltage test conditions in tabular form.

Table 4

SN74LS197 OUTPUT VOLTAGE TEST CONDITIONS

Count/Load	Clear	Inputs A B C D	Outputs Q_A Q_B Q_C Q_D
1	1	CLOCKED OPERATION	1 1 1 1
0	1	1 1 1 1	1 1 1 1
1	0	X X X X	0 0 0 0
0	1	0 0 0 0	0 0 0 0

c. Time Tests

All of the propagation delay measurements specified in the TI TTL Data Book specification sheet were performed. The tests were divided into four categories, depending upon the reference input, as follows:

(1) Propagation time from clock to output
(2) Propagation time from input to output
(3) Propagation time from count/load to output
(4) Propagation time from clear to output

To test the propagation time from the clock to the output, the device was loaded to a count such that when the clock pulse occurred the output being tested would

switch from a low to a high state. This procedure was repeated to test outputs switching from the high to the low state also. The delay from the A, B, C, and D inputs to the outputs was measured by setting the count/load to a low state and then pulsing the data input being tested. This was done for outputs switching both to the high and the low states. The propagation delay between the count/load and output was obtained by setting a logic state at an input and shifting that data through to its corresponding output by driving the count/load into the low state with the reference pulse. The output must be of the opposite state from the input, prior to application of the reference pulse to the count/load, so that the new output pulse can be detected. This measurement was also made for the output switching to both the high and the low states. The propagation delay from the clear to the output was tested by setting the output under test high and then driving the clear low. Due to the function of the clear, this measurement can be obtained only for outputs switching from high to low. These time tests were performed with a TTL load equivalent to a fanout of 10 applied to the outputs.

3. MM74164 8-BIT PARALLEL OUT SHIFT REGISTER

a. Circuit Operation

This CMOS 8-bit shift register has parallel output and serial shift input. Data are serially shifted in and out of the 8-bit register with the positive going edge of the clock. Each bit of register has a parallel output. Table 5 illustrates the truth table for this circuit; t_n is the time before the clock pulse and t_{n+1} is the time after the clock pulse. Q_A is the parallel output from the first bit.

Table 5

MM74C164 TRUTH TABLE

t_n		t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

All the bits may be cleared by applying a low state to the clear input.

b. DC Parametric Tests

The following dc parameters were tested on this device:

(1) High state output voltage
(2) Low state output voltage
(3) High state input current
(4) Low state input current
(5) Supply current

The parametric conditions used to perform these tests (as well as those for the other CMOS device) were taken from the National Semiconductor CMOS Integrated Circuit book.

Threshold voltage shift measurements for individual transistors within these devices could not be made due to the inability to isolate individual transistors. The low level output voltage was checked using four different input conditions:

(1) Input A low, input B high, 8 clock pulses
(2) Input A high, input B low, 8 clock pulses
(3) Input A low, input B low, 8 clock pulses
(4) Clear low

The high level output voltage was checked by setting inputs A and B high and clocking this input through the 8 bits. All output voltage measurements were made after each clock on the appropriate bits and with the proper sink/source current applied. The input current measurements were made for input voltages applied to both inputs, the clock, and the clear, individually. Supply current measurements were taken with the inputs in both the high and low states.

c. Time Tests

Four types of time tests were performed on these devices:

(1) Propagation time from clock to output $\left(t_{pL-H}\right)$
(2) Propagation time from clock to output $\left(t_{pH-L}\right)$
(3) Rise time of output pulse
(4) Fall time of output pulse

Each test was conducted first with one input held high and the other input pulsed and then vice versa. Only alternate bit outputs were considered when performing these measurements.

4. MM74C163 BINARY COUNTER

a. Circuit Operation

This is a CMOS 4-bit counter in which all the bits are programmable and a ripple carry is available for cascading. When the load input is set low, the bits are set to the logic states on inputs A, B, C, and D after the next clock. Similarly, a low level at the clear input sets the bits low after the next clock. Both enable inputs T and P must be high for clocking. Table 6 illustrates the truth table for this circuit.

Table 6

MM74C163 TRUTH TABLE

t_n					t_{n+1}
Clr	T	P	Inputs A, B, C, D	Load	Q_A, B, C, D
0	X	X	X	X	0
1	X	X	1	0	1
1	X	X	0	0	0
1	1	1	X	1	Counting

Note: X = doesn't care

b. DC Parametric Tests

The dc tests for this device were the same as for the shift register except for the addition of a check on the P and T enable inputs. As with previous devices, each test was performed under the various input conditions which achieve the desired output, as applicable.

c. Time Tests

Propagation delay measurements were obtained from the clock to outputs Q_A, Q_B, Q_C, Q_D, and the ripple carry. This was accomplished for outputs transitioning from high to low and from low to high.

SECTION III

TRANSIENT IONIZING RADIATION TESTS

All four device types were subjected to a short pulse (∿ 20 ns width) dose-rate environment while in a dynamic mode, using AFWL's Febetron 705 flash X-ray (FXR) machine. The purpose of this testing was to study logic upset under transient radiation conditions. Four of each device type were used for these tests; three devices for irradiation and one for a control. Each device was electrically characterized prior to irradiation to obtain a preirradiation data base. The devices were then characterized after various radiation levels to check for permanent damage effects. Dynamic failure was defined as a change in the logic state of a bit due to the radiation. Figure 3 shows the schematic of the general test setup used for the transient radiation logic upset tests. The TTL load is used to simulate an approximate fanout of 10. R_L equals 200Ω for the standard SN7491A and 800Ω for the low power Schottky SN74LS197. A 0.1 μF capacitor is applied in parallel with the power supply to hold it constant during the radiation pulse. Fifty ohm terminators were used at the oscilloscopes to reduce reflections down the coaxial cables. LH0033C unity gain line drivers were used with a divide-by-two resistive divider network to provide the necessary drive for the 50 ohm terminated cables. The devices were irradiated with the output in the high, low, and transition states to find the worst case failure mode. Figure 4 shows the input and output conditions for each of the four device types during testing. The TTL devices were clocked at 5 MHz, while the CMOS devices were clocked at 500 kHz.

Table 7 is a list of the failure levels for each of the device types. Although the failure was assumed to occur somewhere between the highest level at which the devices passed and the level at which they failed, the table presents the highest radiation levels in which all four devices of each type did not experience logic upset.

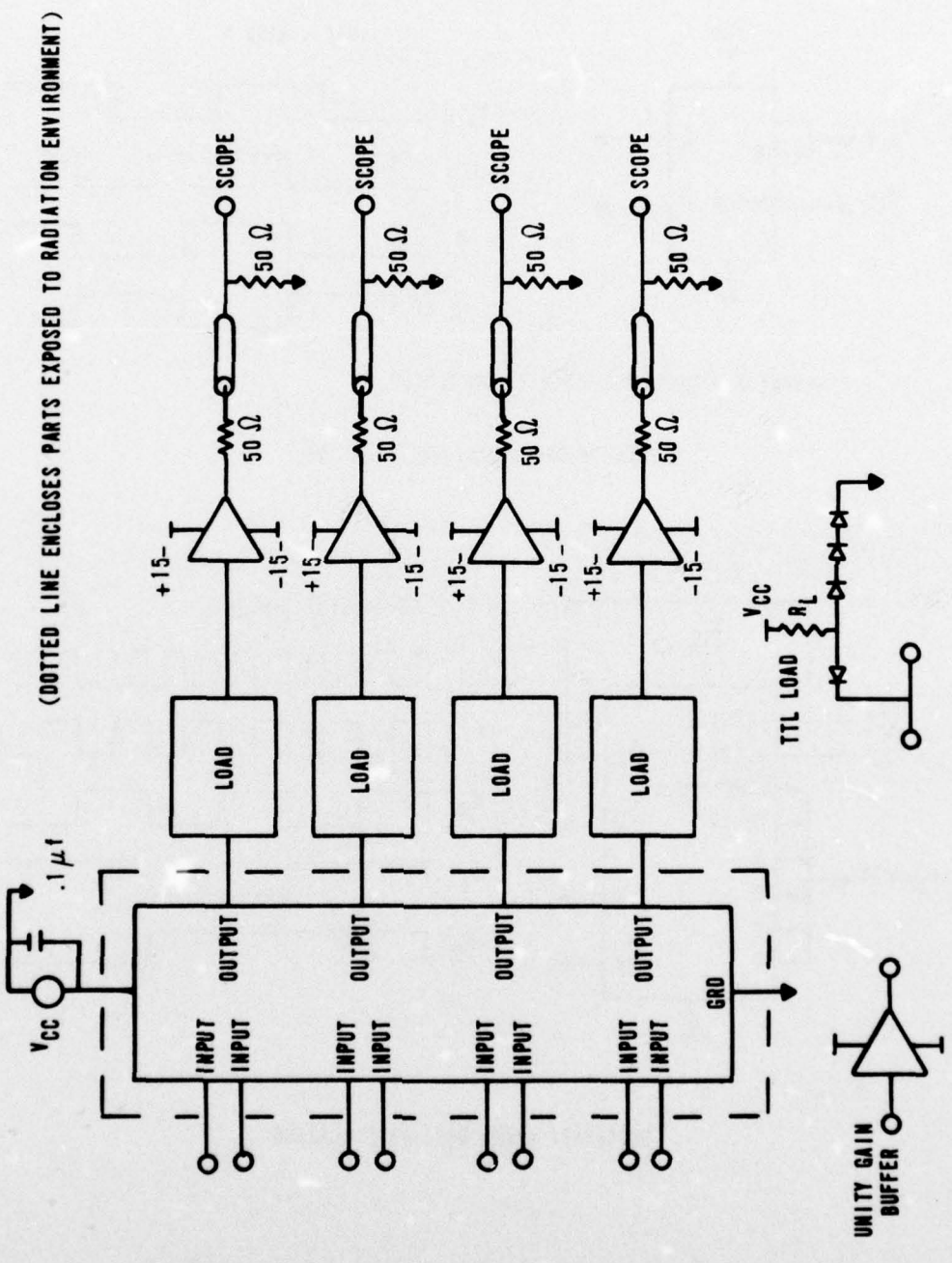
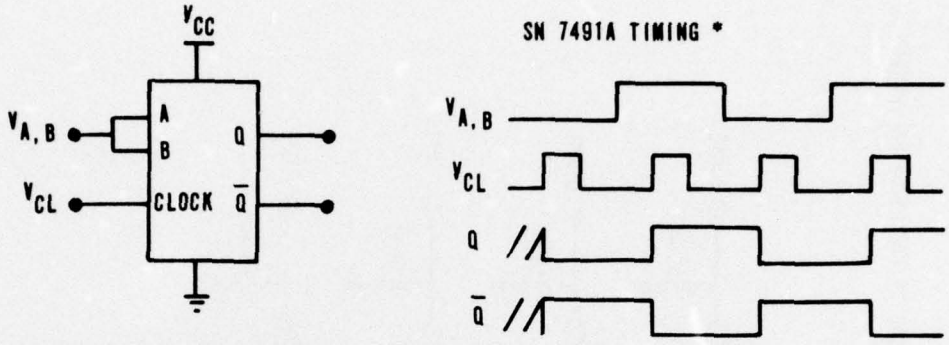
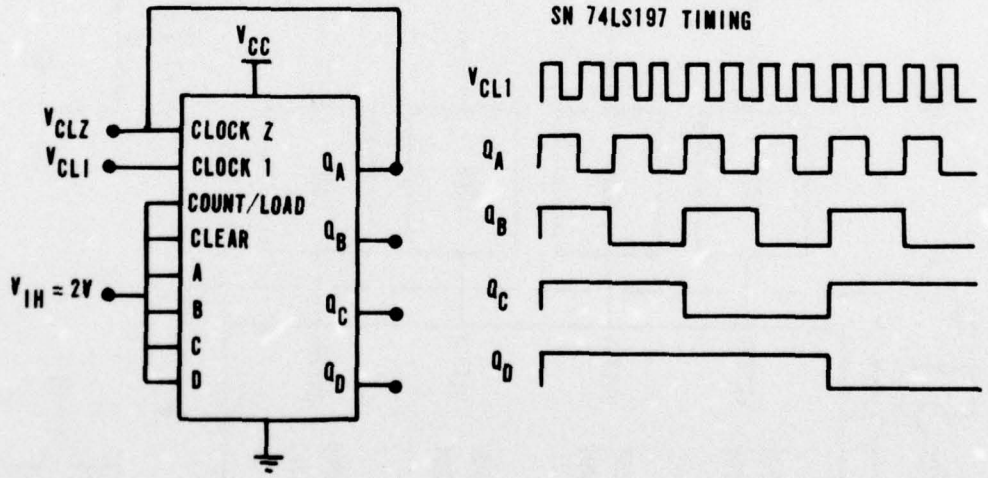


Figure 3. Transient Radiation Test Schematic



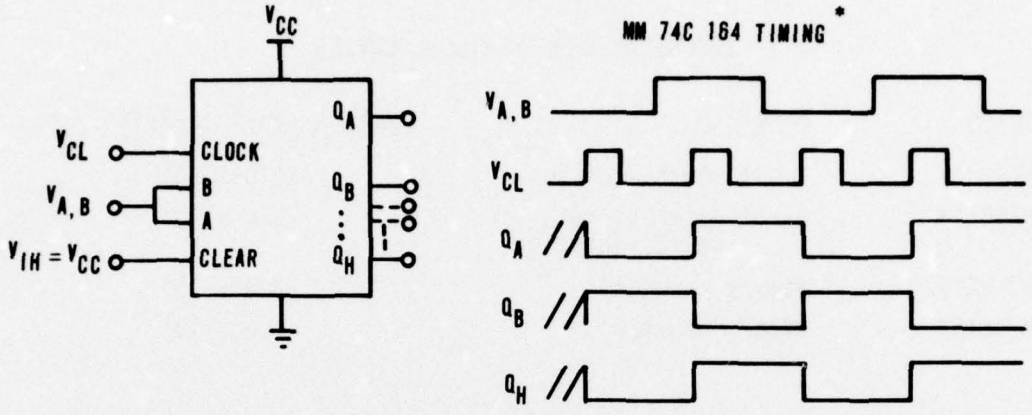
* ASSUMING 8 CLOCK PULSES HAVE OCCURRED

SN7491A GAMMA DOSE-RATE BIASING



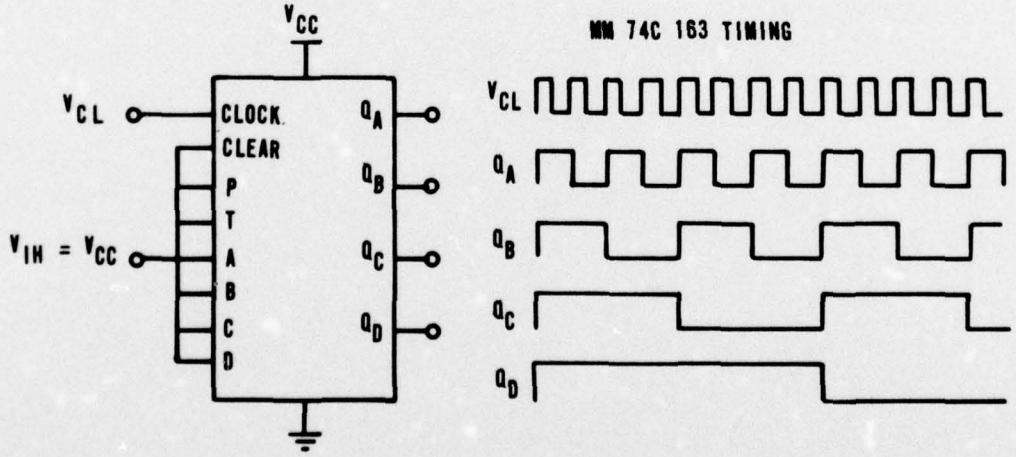
SN74LS197 GAMMA DOSE-RATE BIASING

Figure 4. Circuit Biasing During Transient Tests



* ASSUMING 8 CLOCK PULSES HAVE OCCURRED

MM74C164 GAMMA DOSE-RATE BIASING



MM74C163 GAMMA DOSE-RATE BIASING

Figure 4 (cont). Circuit Biasing During Transient Tests

Table 7

TRANSIENT UPSET FAILURE LEVELS

Device	Function	Failure Level (Rads(Si)/sec)
SN7491A	8-bit shift register	2.0×10^8
MM74C164	8-bit parallel out shift register	2.0×10^8
SN74LS197	Binary counter	3.0×10^8
MM74C163	Binary counter	2.0×10^8

SECTION IV

NEUTRON RADIATION TESTS

Fifteen SN7491A and fifteen SN74LS197 circuits were irradiated at the Sandia Pulsed Reactor (SPR) in incremental neutron fluence levels. After each incremental neutron fluence was reached, the devices were electrically tested on the Fairchild 5000/5800. The cumulative neutron fluence levels at which the devices were electrically tested are shown below.

2.8×10^{12} n/cm^2

7.8×10^{12} n/cm^2

4.1×10^{13} n/cm^2

1.4×10^{14} n/cm^2

4.6×10^{14} n/cm^2

7.3×10^{14} n/cm^2

These fluence levels are 1 MeV equivalent. All 30 devices were irradiated together with no electrical bias applied to them. One of each device type was not irradiated for use as a control device.

Figures 5 through 13 and figures 14 through 22 illustrate the electrical parametric degradation resulting from neutron fluence damage on the SN7491A shift register and the SN74LS197 binary counter, respectively. The data are plotted for a device from each circuit type which is representative of the average.

Figures 5 and 14 are plots of the logic "1" and logic "0" output voltages versus neutron fluence. The output voltage measurements were made with load currents, which simulate a fanout of 10, applied to the outputs. The output low voltage failure threshold was defined as 0.8 volt, and the output high voltage was defined as 2.0 volts.

Both the SN7491A and the SN74LS197 failed between 1.4×10^{14} n/cm^2 and 4.6×10^{14} n/cm^2. The failure resulted from the output low voltage becoming

greater than 0.8 volt. This is caused by the neutron induced beta degradation of the output transistors of the device. As beta decreases on these transistors, less current can be sunk by the transistors before they enter the linear region of operation. When the current, which can be sunk, becomes less than the fanout of 10 sink current, the output transistors' collector emitter voltage (V_{CE}), which equals the output voltage, will increase suddenly as a result of the linear operation of the transistors. This is illustrated in figures 5 and 14.

Figures 6 and 7 are plots of the output drive and sink current for the SN7491A. Similarly, figures 15 and 16 are plots of the output drive and sink current for the SN74LS197. These currents also decrease as a result of the neutron induced beta degradation of the circuit output transistors. The information is valuable for determining the fanout capability of these devices for a given neutron fluence.

Figures 8, 9, 10, and 11 and figures 17, 18, 19, and 20 show the neutron induced change in the short circuit output current, supply current, and input current of the SN7491A and SN74LS197, respectively.

Figures 12 and 13, and figures 21 and 22 illustrate the neutron induced changes in propagation delay time of the SN7491A and the SN74LS197, respectively. The relative changes of the propagation delay times are more important than the actual values, since the capacitive loading of the Fairchild 5000/5800 is uncertain.

The information contained in these figures characterizes the neutron fluence response of these TTL sequential logic circuits very well.

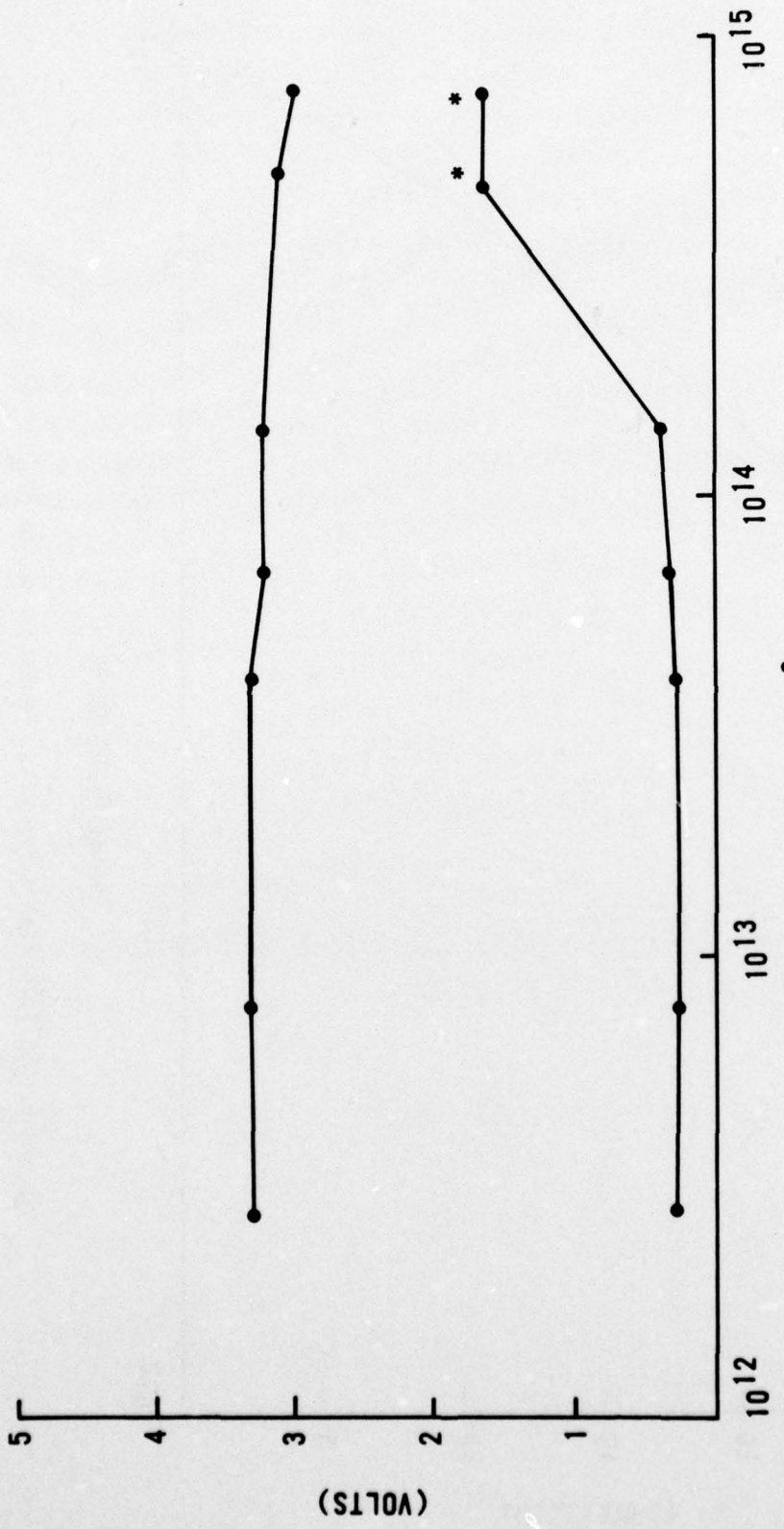


Figure 5. SN7491A Output Voltage vs. Neutron Fluence (*The Fairchild 5000 test system clamps the voltage at 1.63 volts to prevent overvoltage destruction.)

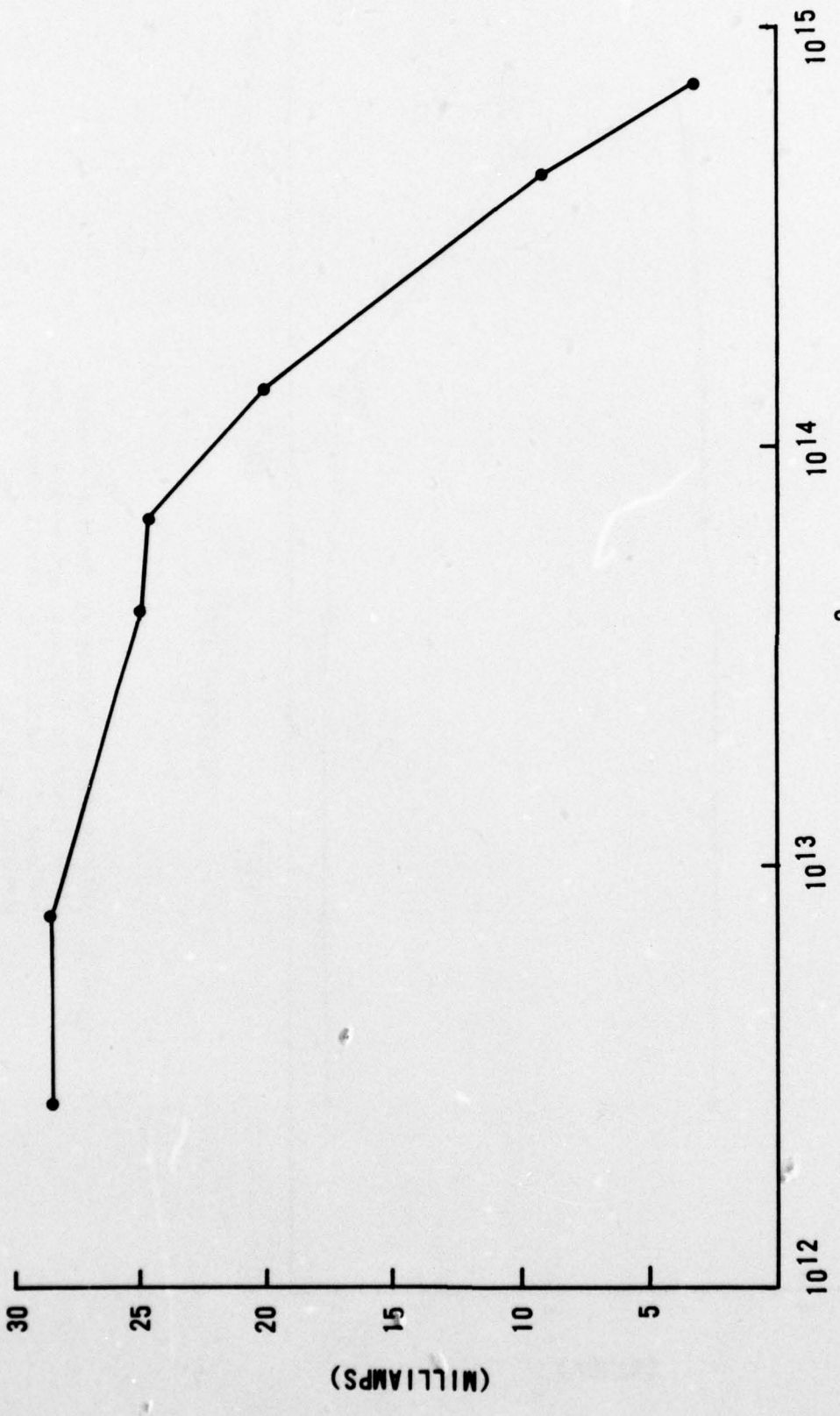


Figure 6. SN7491A Sink Current vs. Neutron Fluence (V_{OL} = .4 V)

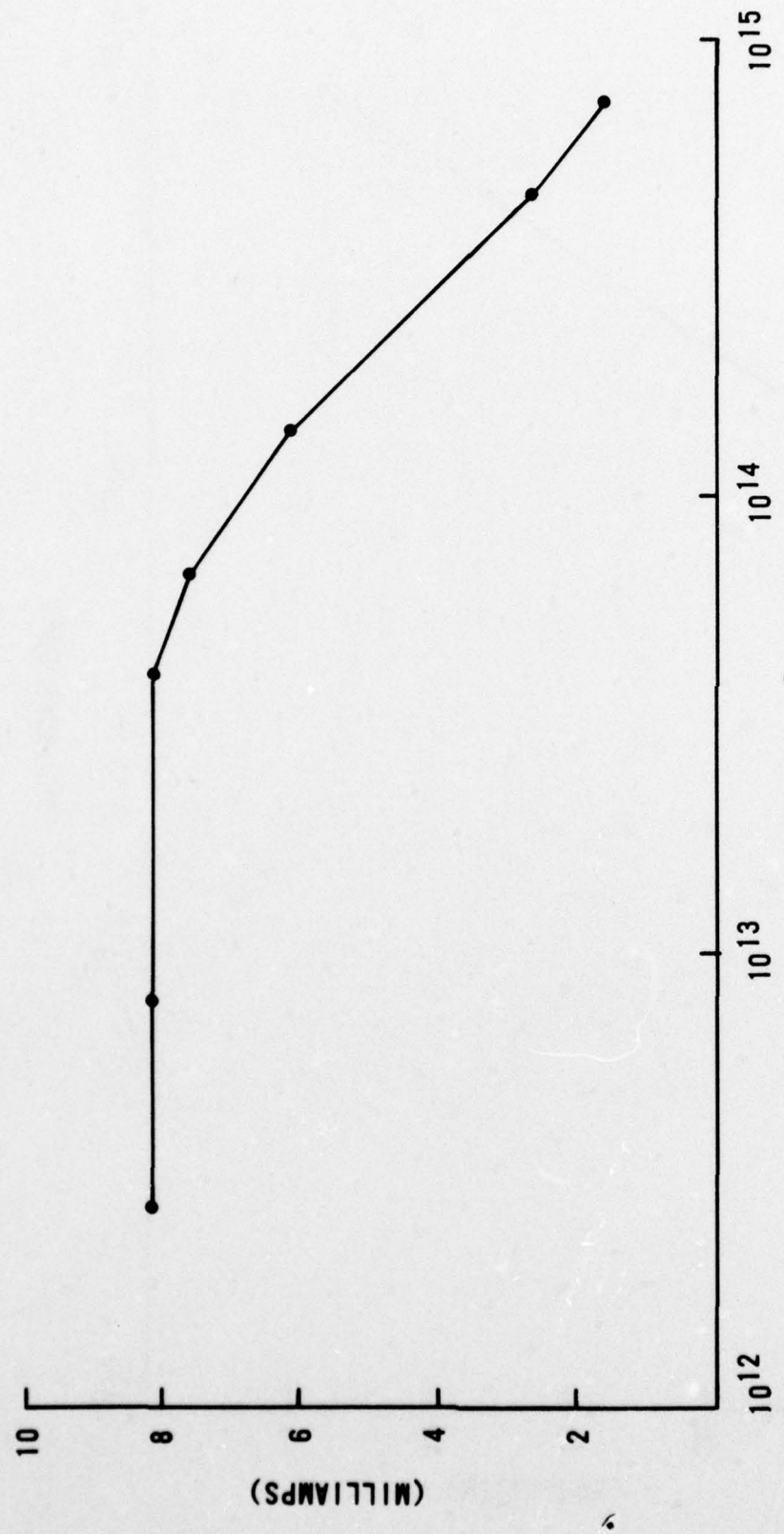


Figure 7. SN7491A Source Current vs. Neutron Fluence (V_{OH} = 2.4 V)

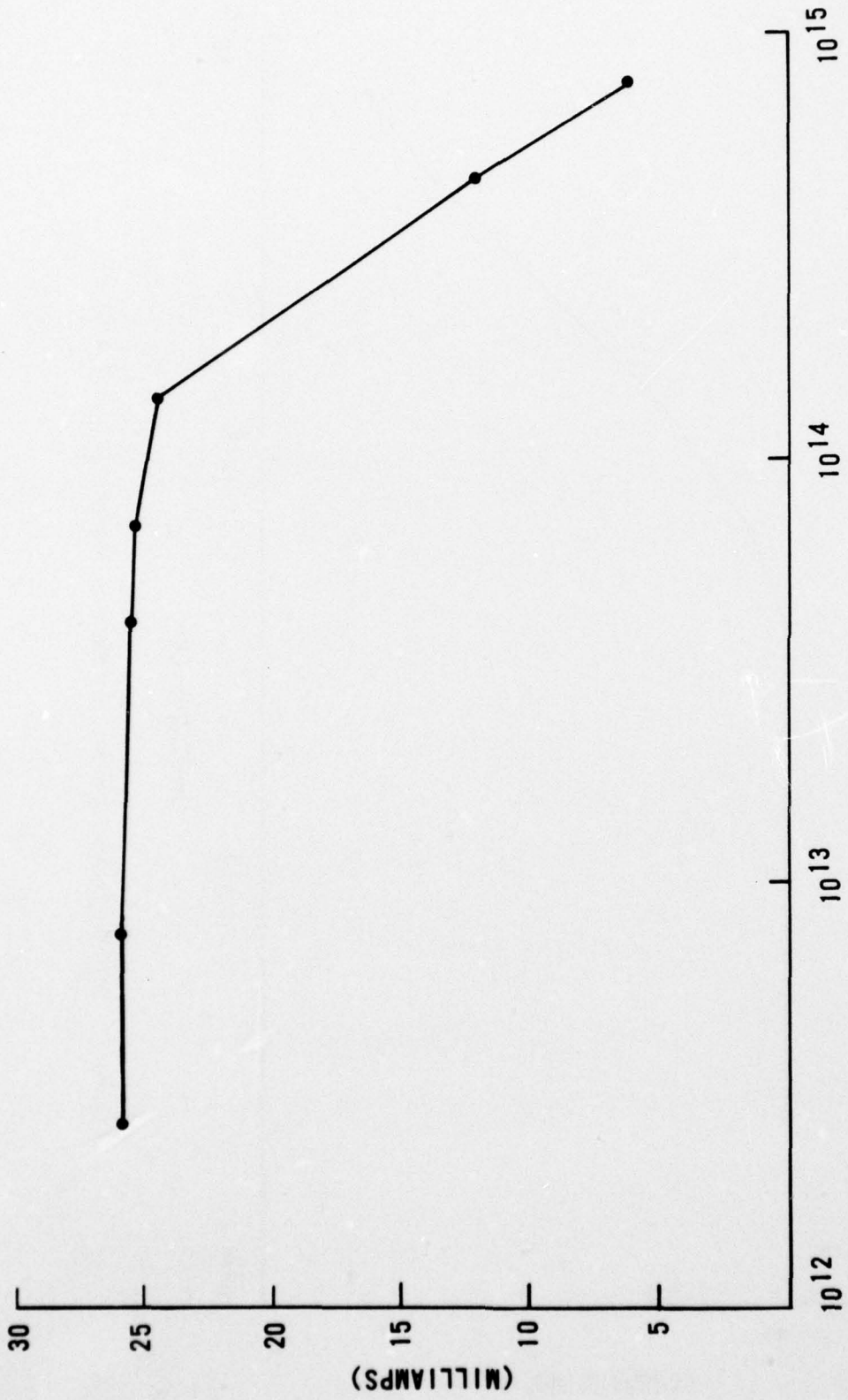


Figure 8. SN7491A Short Circuit Output Current vs. Neutron Fluence

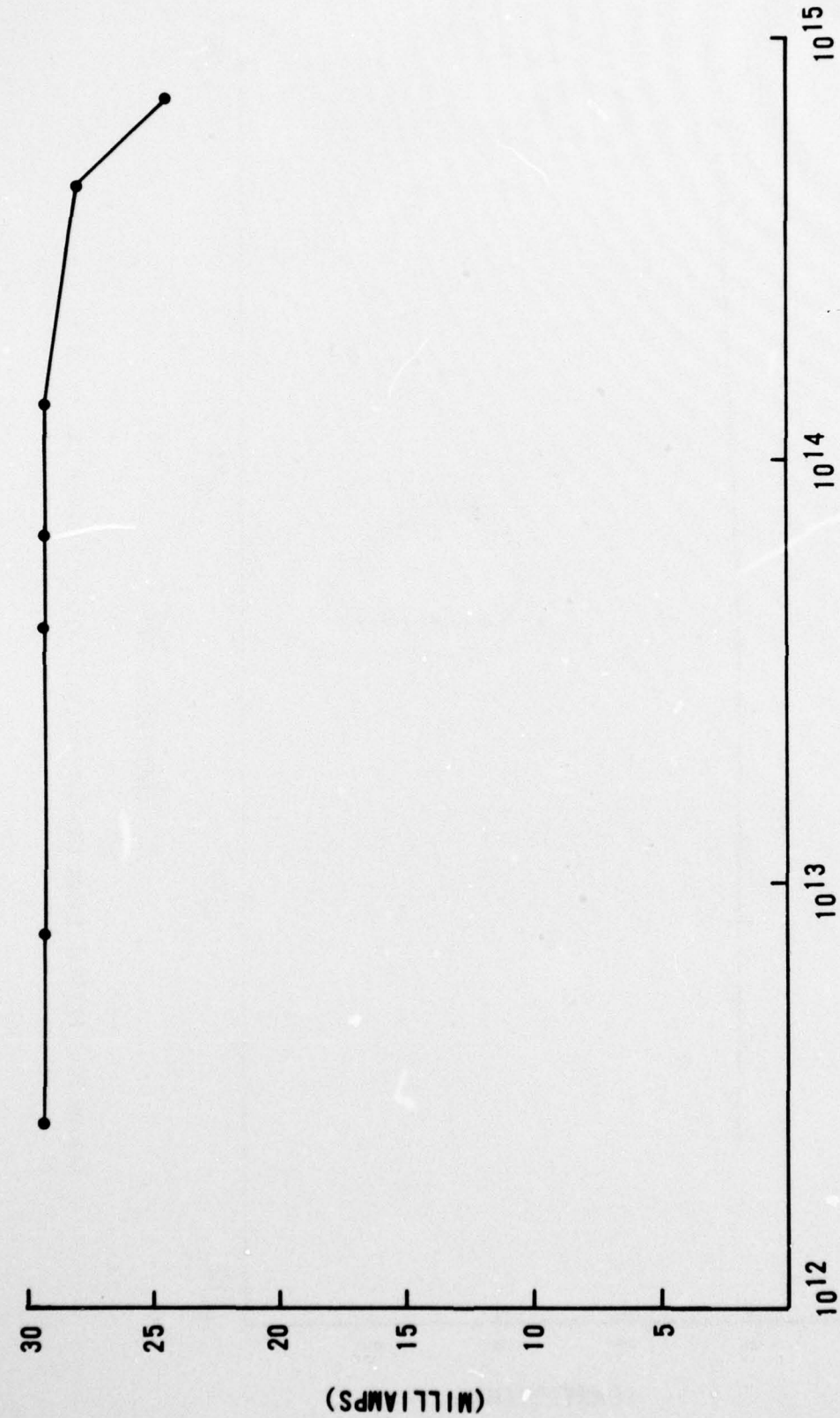


Figure 9. SN7491A Supply Current vs. Neutron Fluence

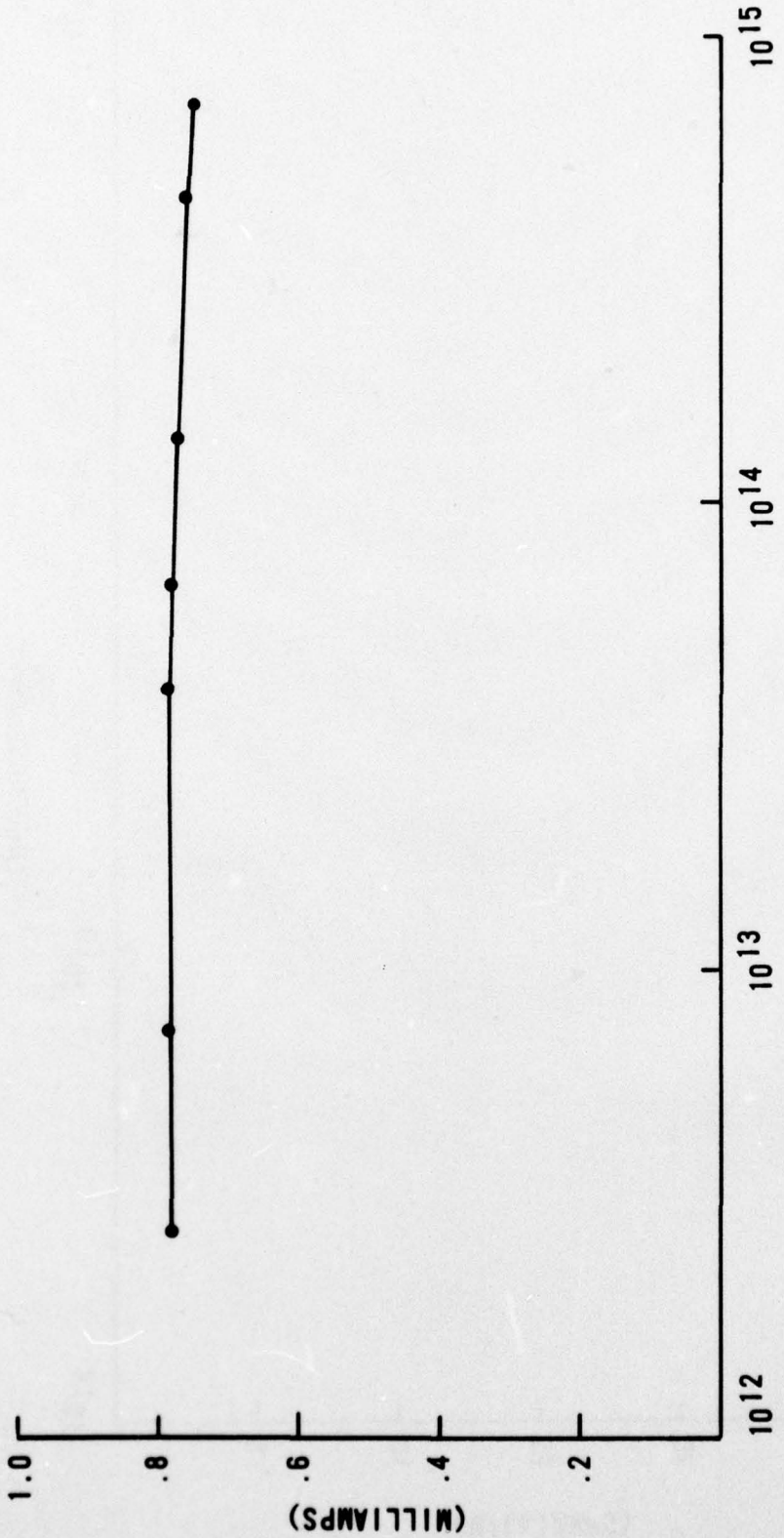


Figure 10. SN7491A Input Low Current vs. Neutron Fluence (V_{IN} = .8 V)

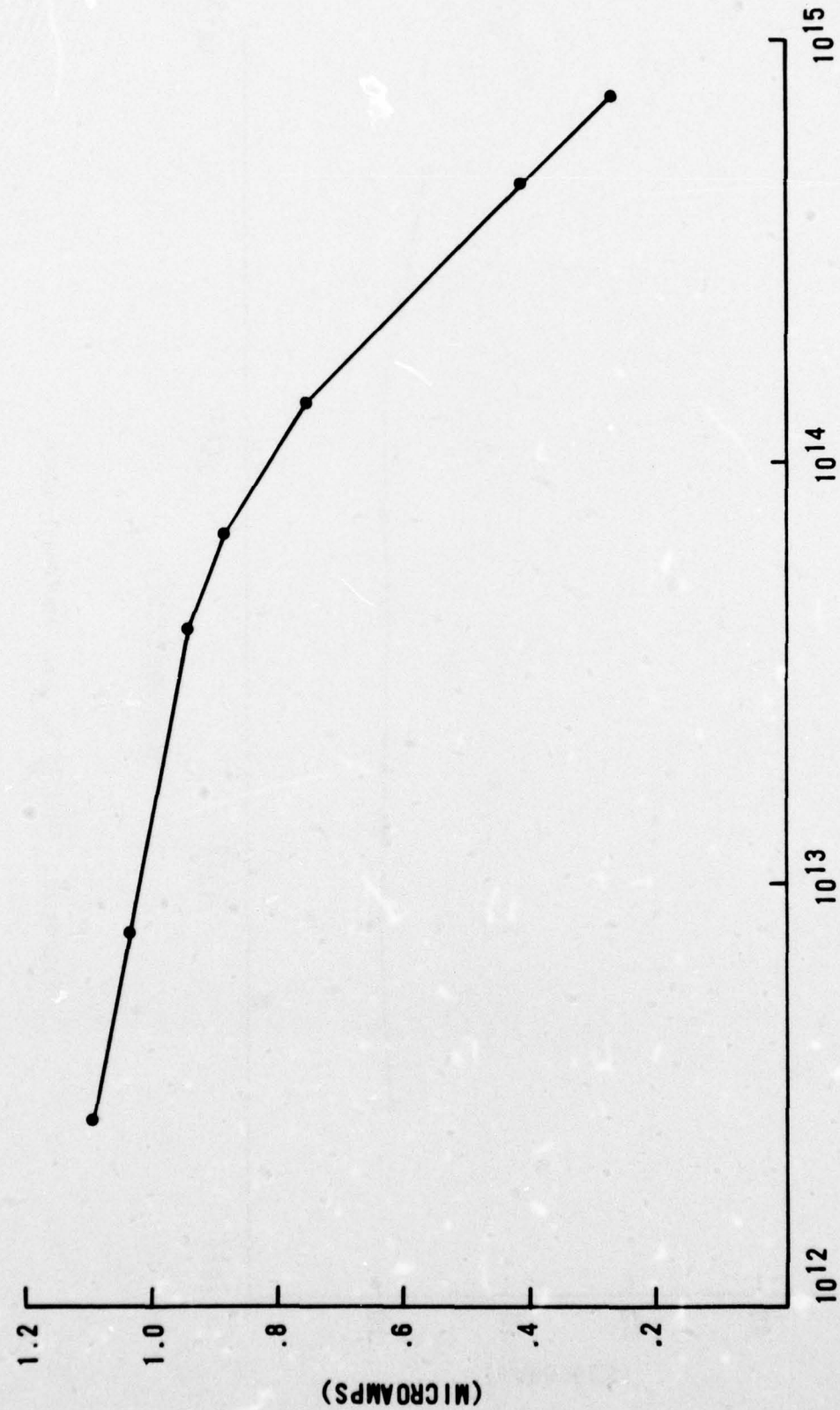


Figure 11. SN7491A Input High Current vs. Neutron Fluence (V_{IN} = 2.4 V)

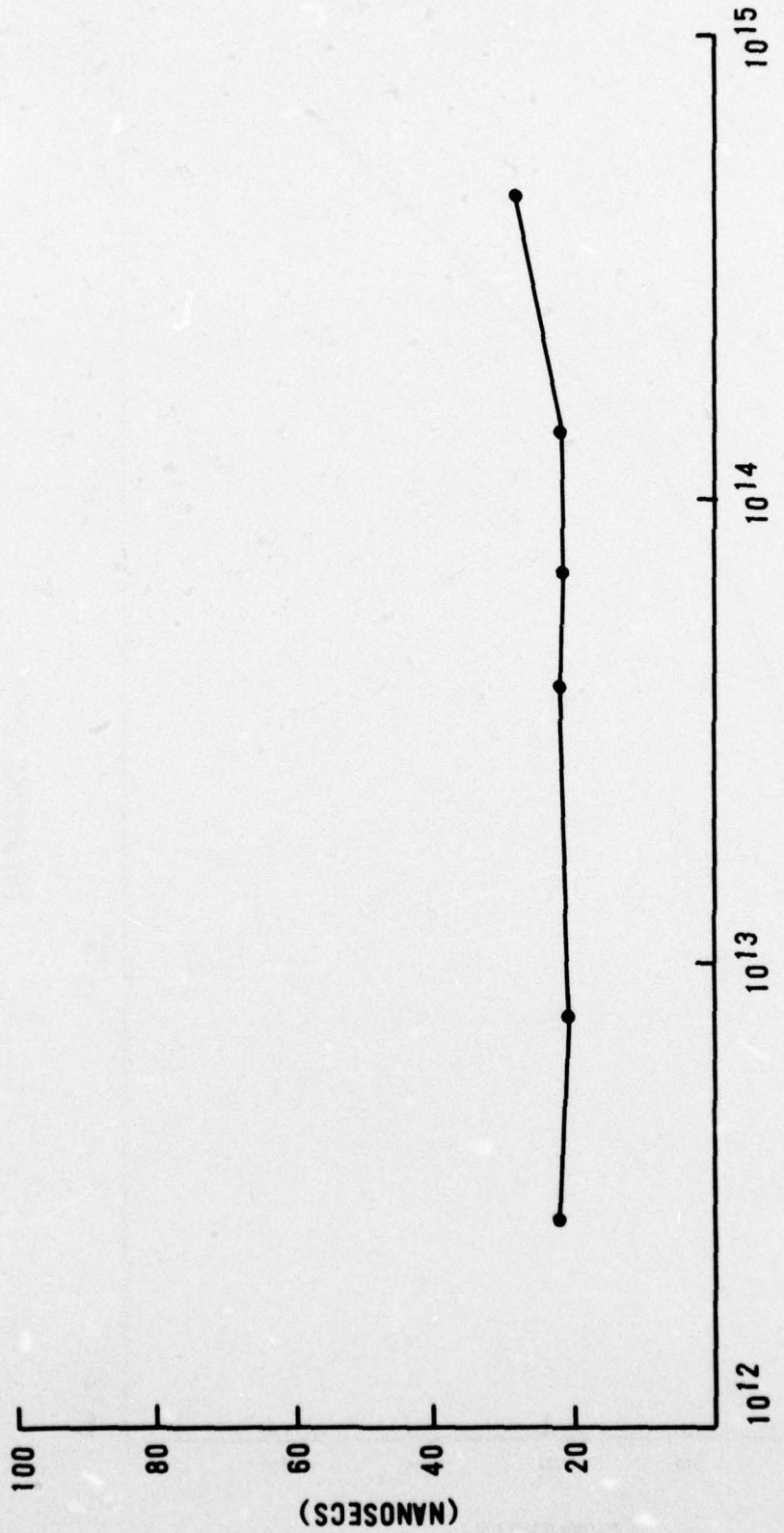


Figure 12. SN7491A t_{PLH} vs. Neutron Fluence

Figure 13. SN7491A T_{PHL} vs. Neutron Fluence

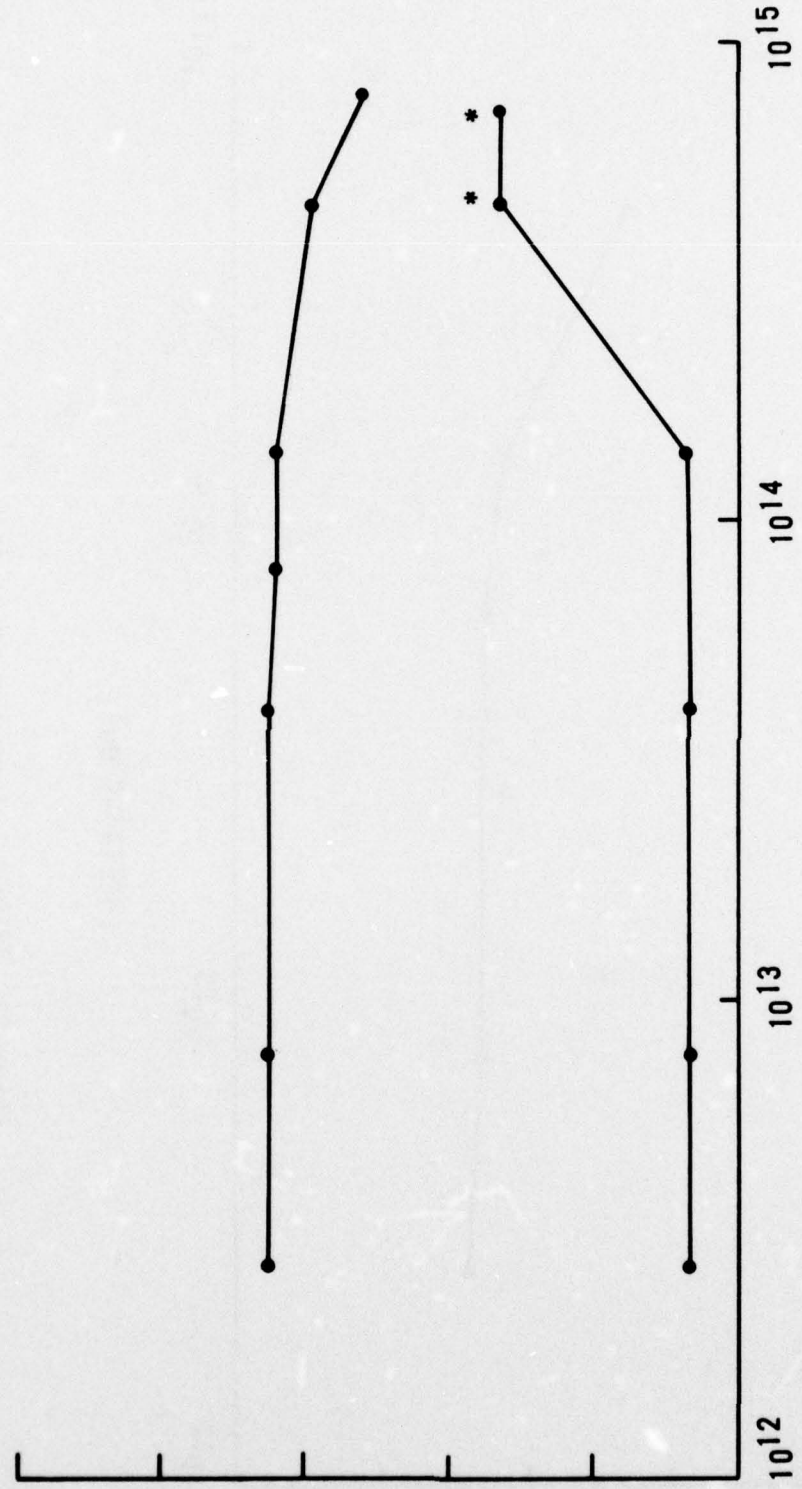


Figure 14. SN74LS197 Output Voltage vs. Neutron Fluence (*The Fairchild 5000 test system clamps the voltage at 1.63 volts to prevent over-voltage destruction.)

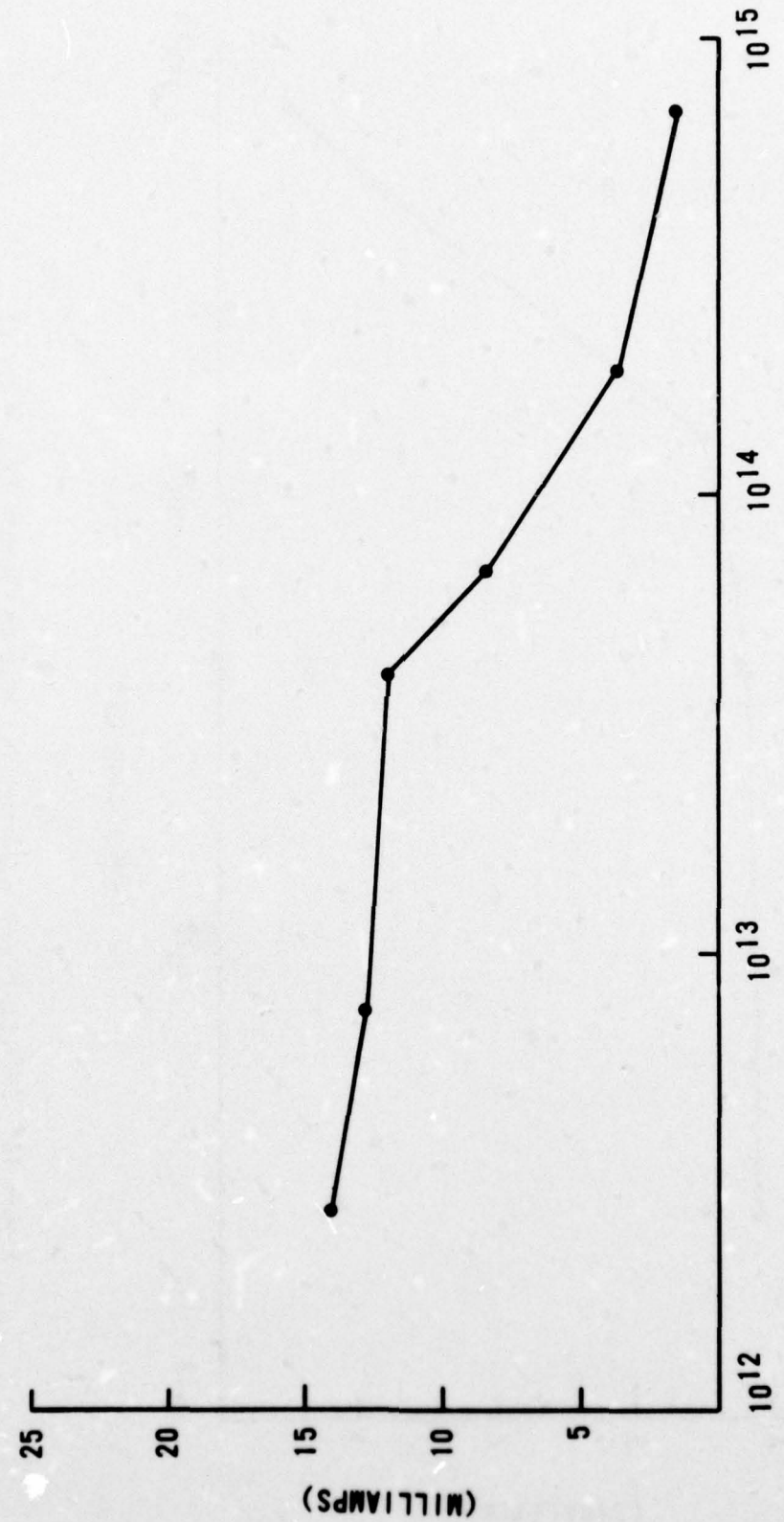


Figure 15. SN74LS197 Sink Current vs. Neutron Fluence (V_{OL} = .5 V)

Figure 16. SN74LS197 Source Current vs. Neutron Fluence (V_{OH} = 2.7 V)

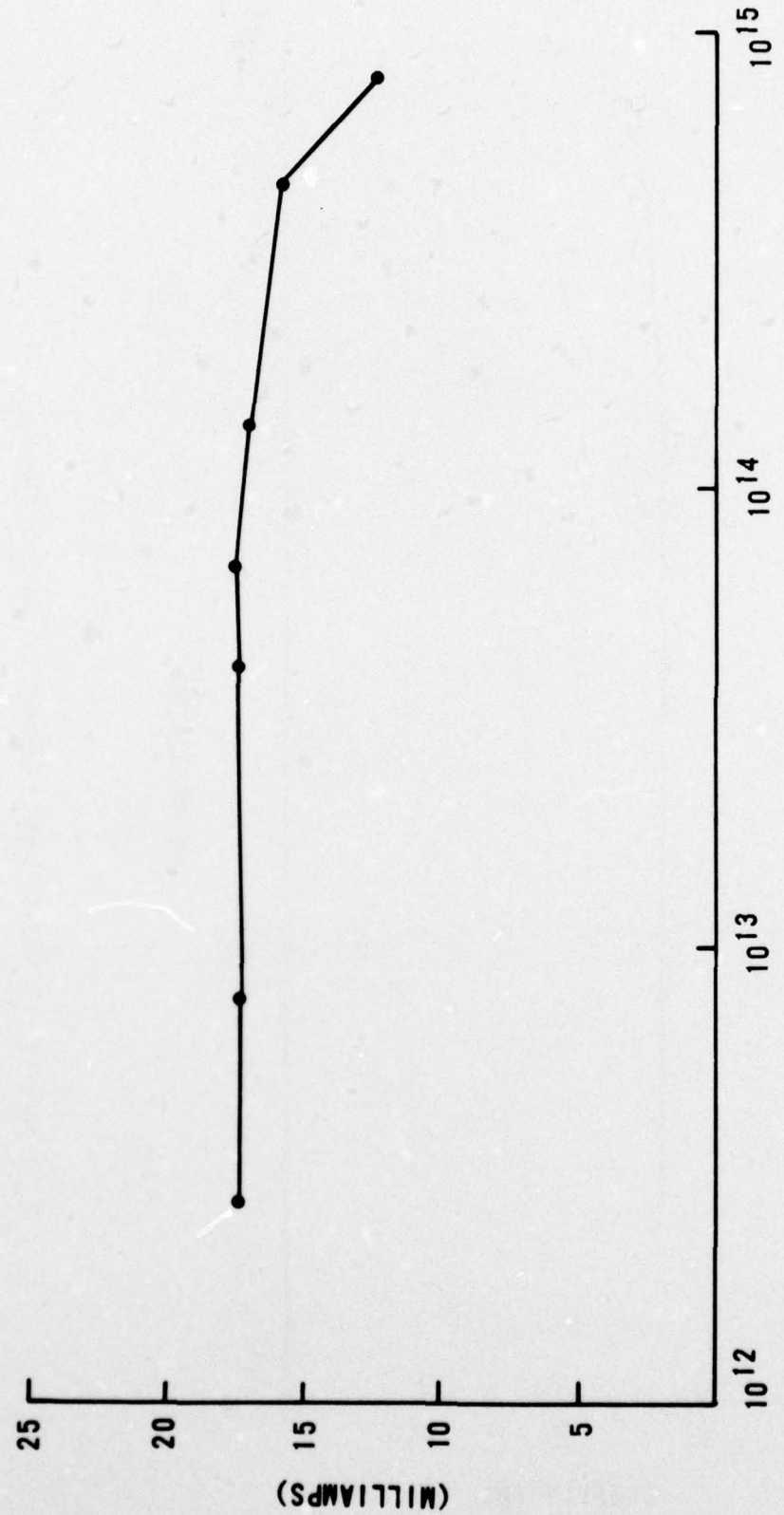


Figure 17. SN74LS197 Short Circuit Output Current vs. Neutron Fluence

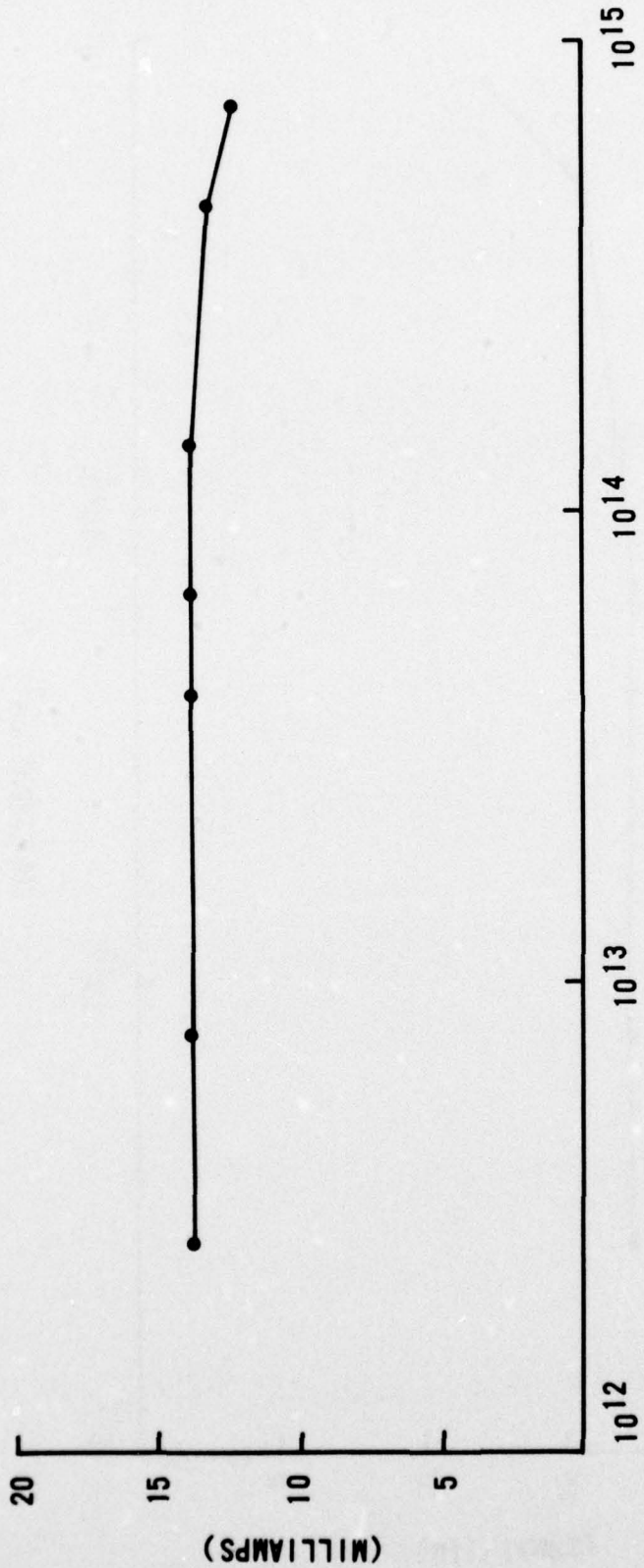


Figure 18. SN74LS197 Supply Current vs. Neutron Fluence

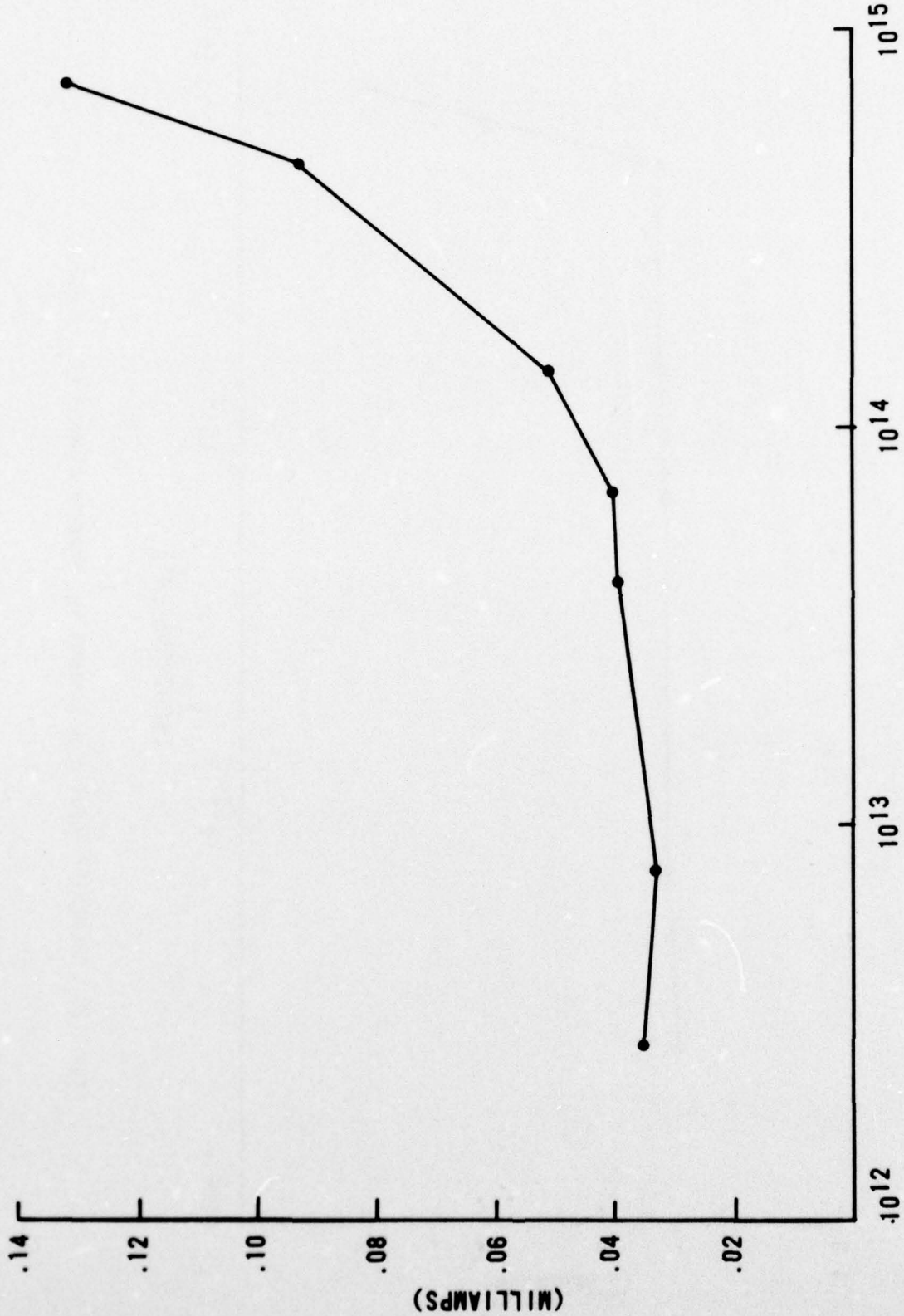


Figure 19. SN74LS197 Input Low Current vs. Neutron Fluence

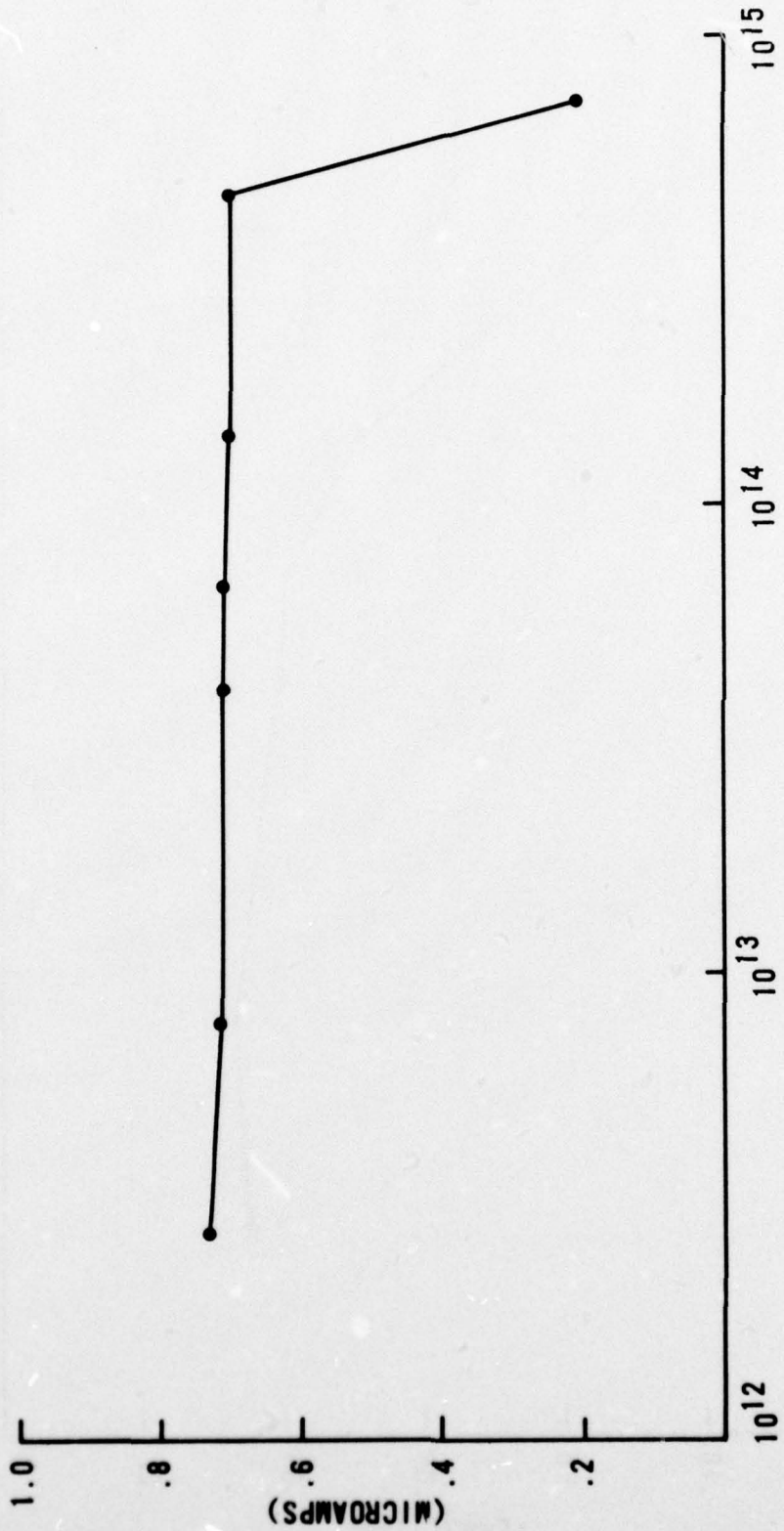


Figure 20. SN74LS197 Input High Current vs. Neutron Fluence (V_{IN} = 2.7 V)

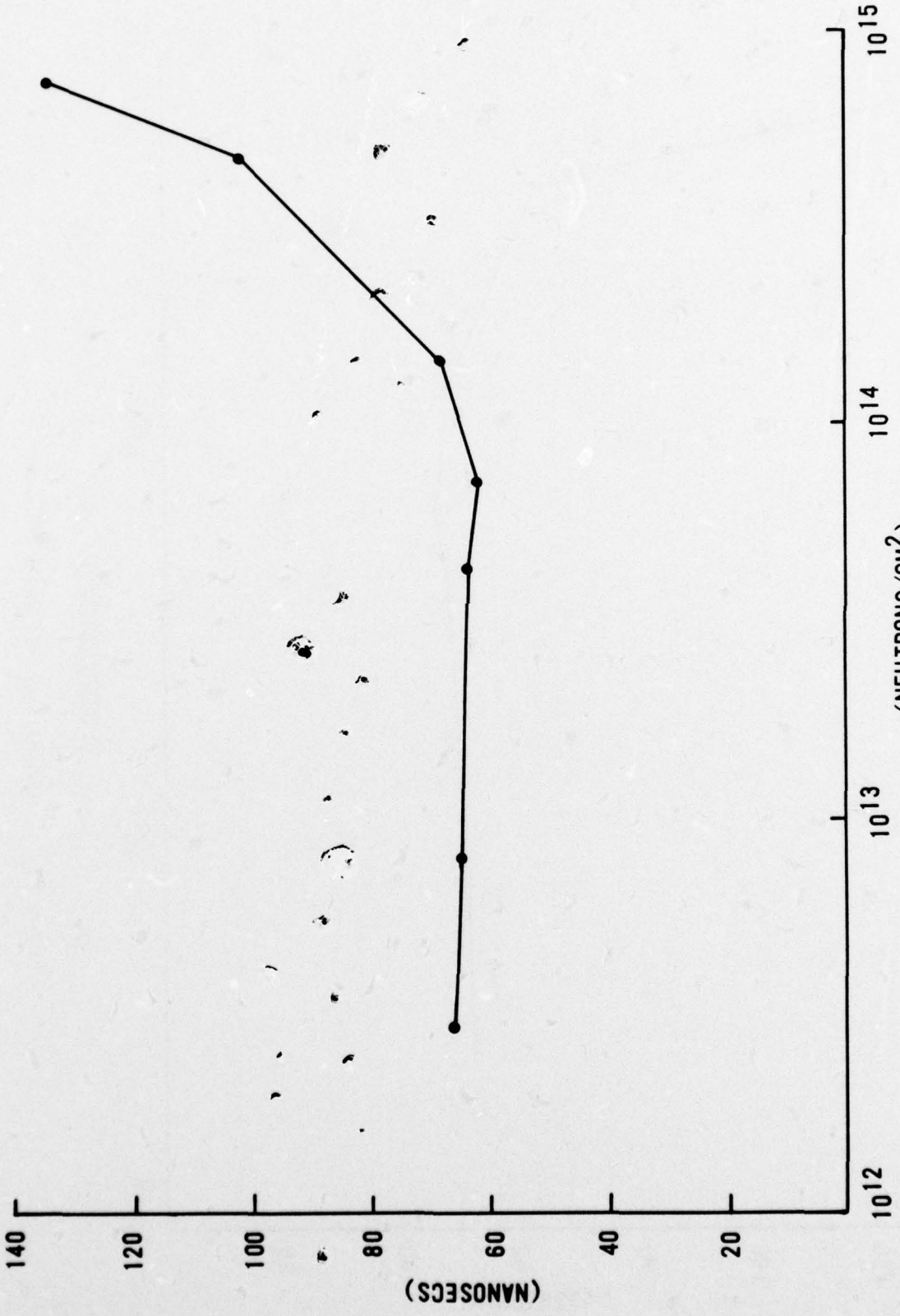


Figure 21. SN74LS197 t_{PLH} vs. Neutron Fluence

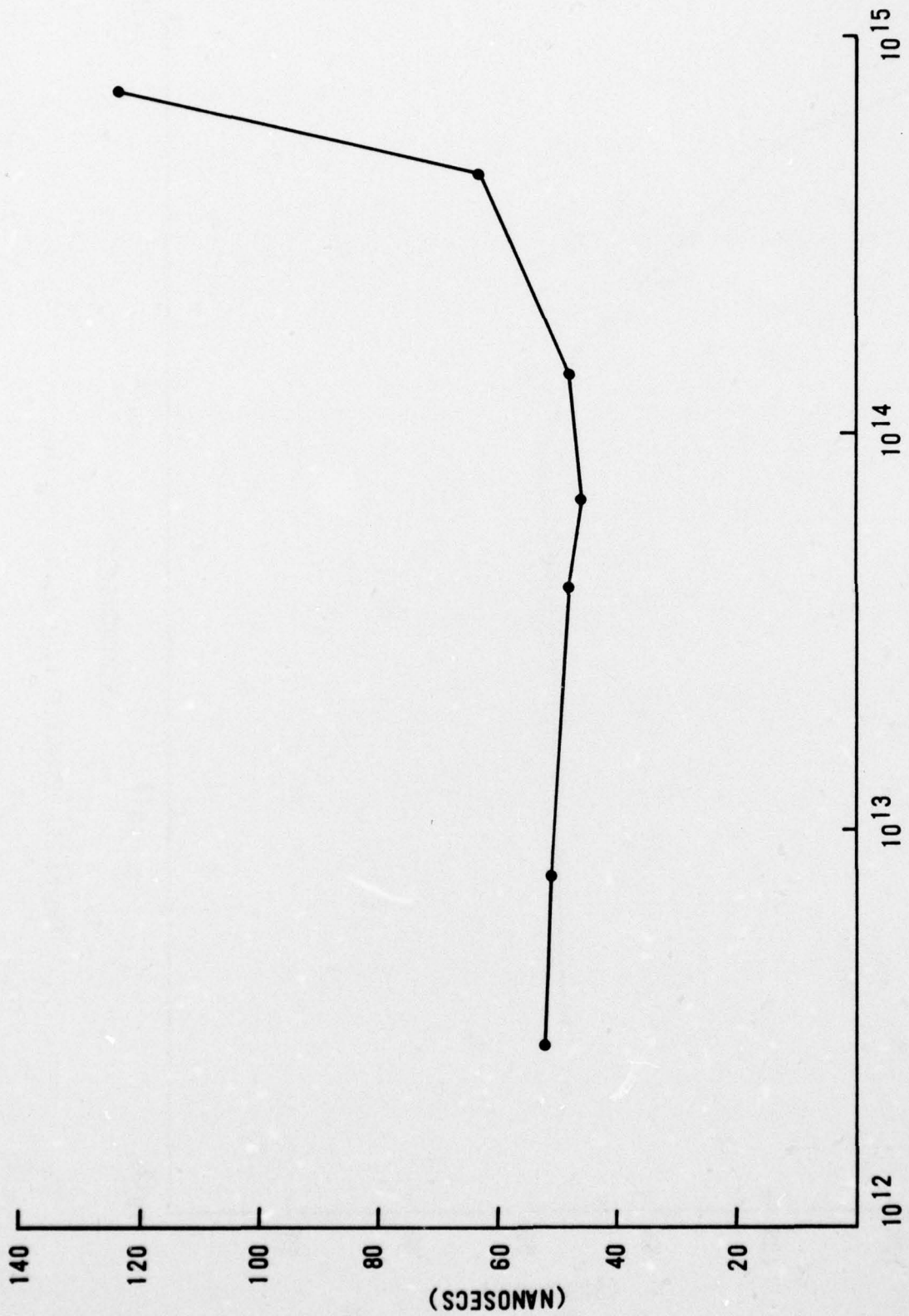


Figure 22. SN74LS197 t_{PHL} vs. Neutron Fluence

SECTION V

TOTAL GAMMA DOSE TESTS

The MM74C164 and MM74C163 were exposed at various levels at the AFWL Co^{60} source for total gamma dose survivability. Fifteen devices of each type were biased with all inputs tied to VCC. The 30 devices were arranged so all devices received equal exposure. After each exposure level, all 30 devices and 2 controls were tested on the Fairchild 5000/5800.

The cumulative total gamma dose exposure levels at which the devices were electrically tested are shown below.

196 rads(Si)
360 rads(Si)
1490 rads(Si)
3956 rads(Si)
6088 rads(Si)

Figures 23 through 26 and figures 27 through 30 illustrate the electrical parametric degradation resulting from total gamma dose damage on the MM74C164 shift register and the MM74C163 binary counter. The data are plotted for a device from each circuit type which is representative of the average.

Figures 23 and 27 are plots of the logic "1" and "0" output voltages versus total gamma dose. Both the MM74C163 and MM74C164 failed to logically operate after 1490 rads(Si). The output voltage levels did not degrade, but the logic outputs failed to switch to the correct state. Figures 24, 25, and 26, and figures 28, 29, and 30 show the total gamma dose induced change in the supply current, t_{PHL}, and t_{PLH} of the MM74C164 and MM74C163, respectively. As shown in the output voltage and supply current plots, the supply current increased significantly when the output voltage failures occurred. The increased supply current (leakage current) and output voltage failures are a result of the radiation indiced n-channel threshold voltage shifts in the CMOS circuits. Since the threshold voltages cannot be measured directly on the circuits, the supply current can be used to indicate threshold voltage shifts and output voltage failures.

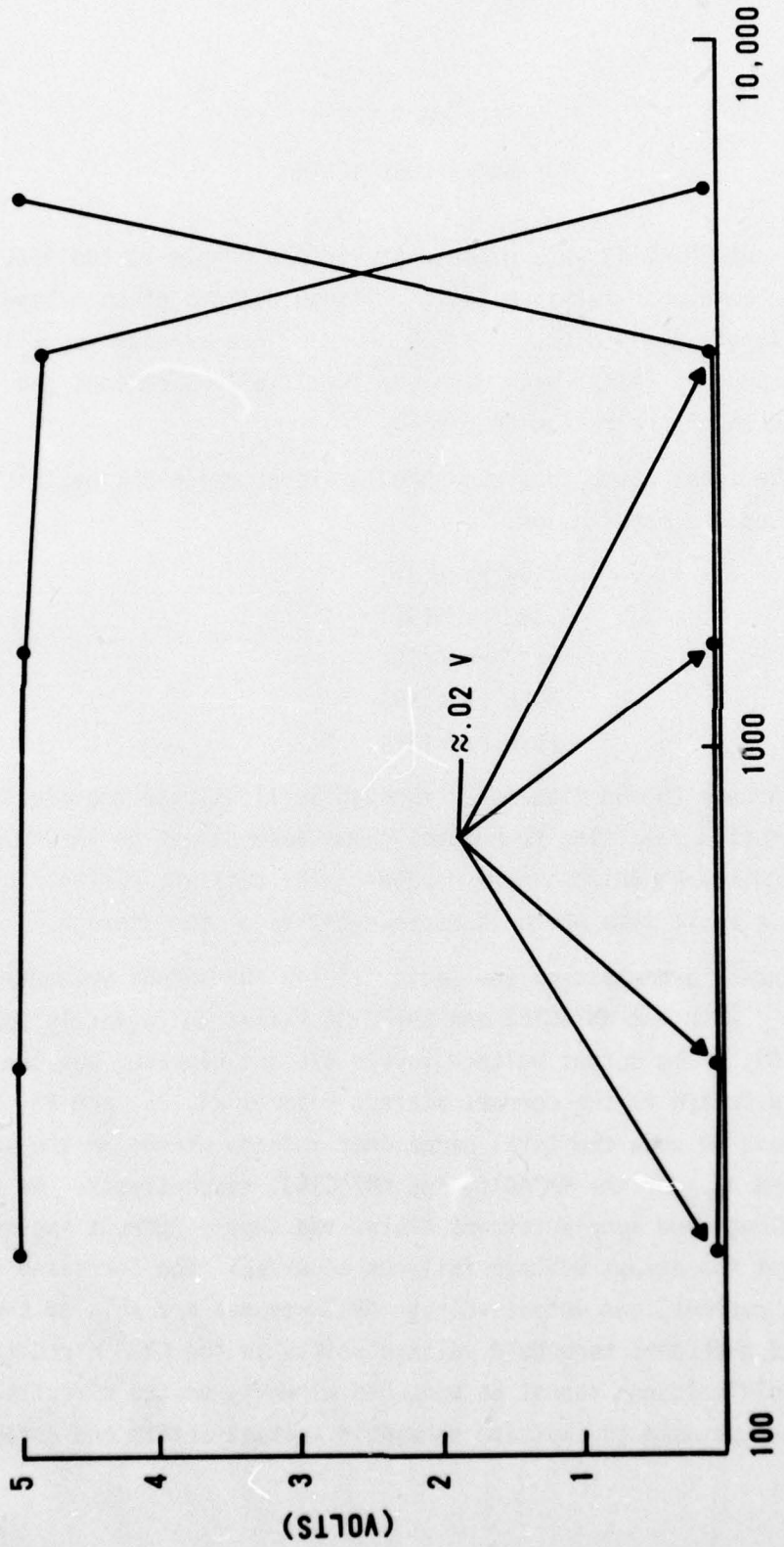


Figure 23. MM74C164 Output Voltage vs. Total Gamma Dose

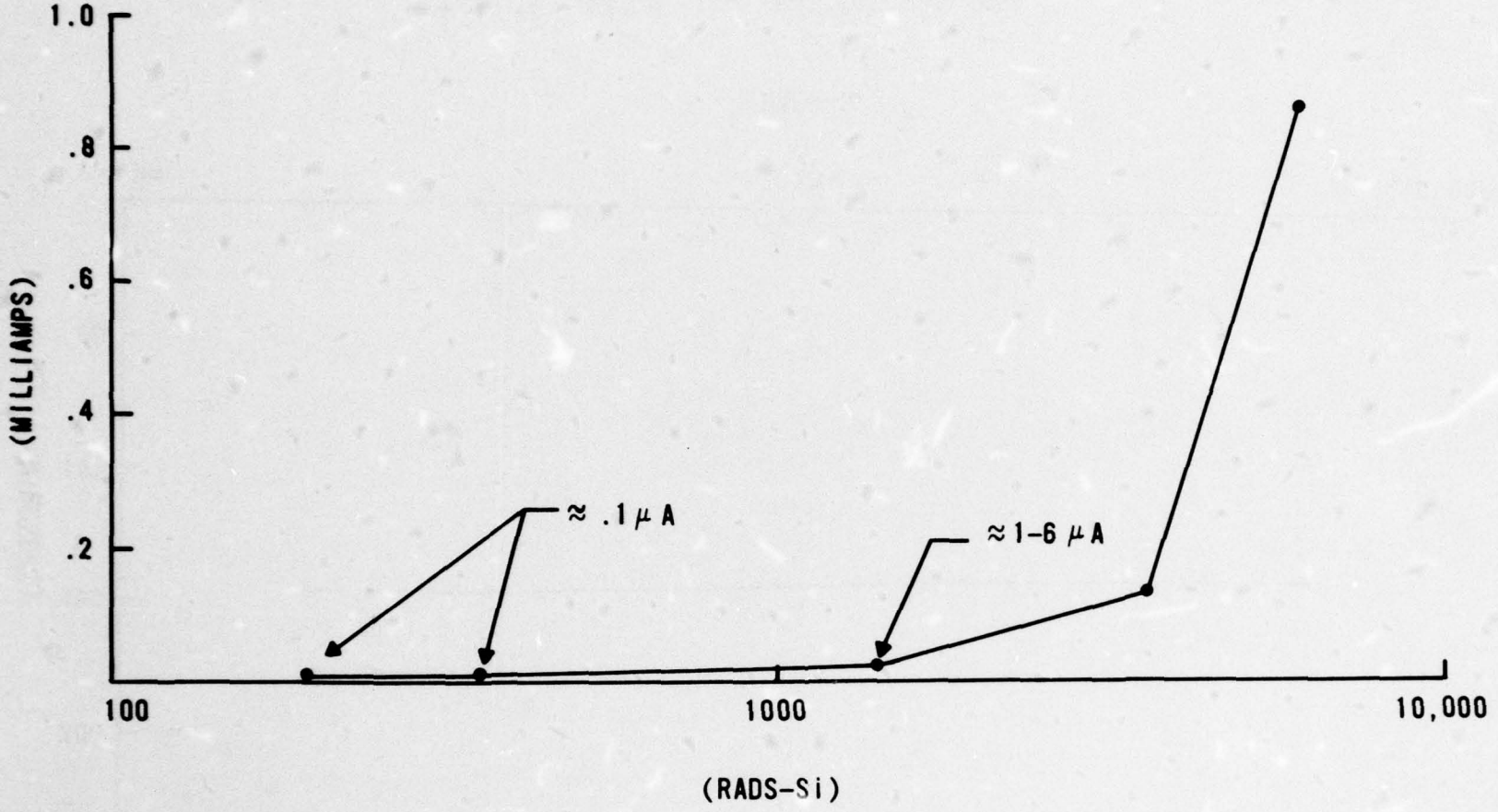


Figure 24. MM74C164 Supply Current vs. Total Gamma Dose

Figure 25. MM74C164 t_{PHL} vs. Total Gamma Dose

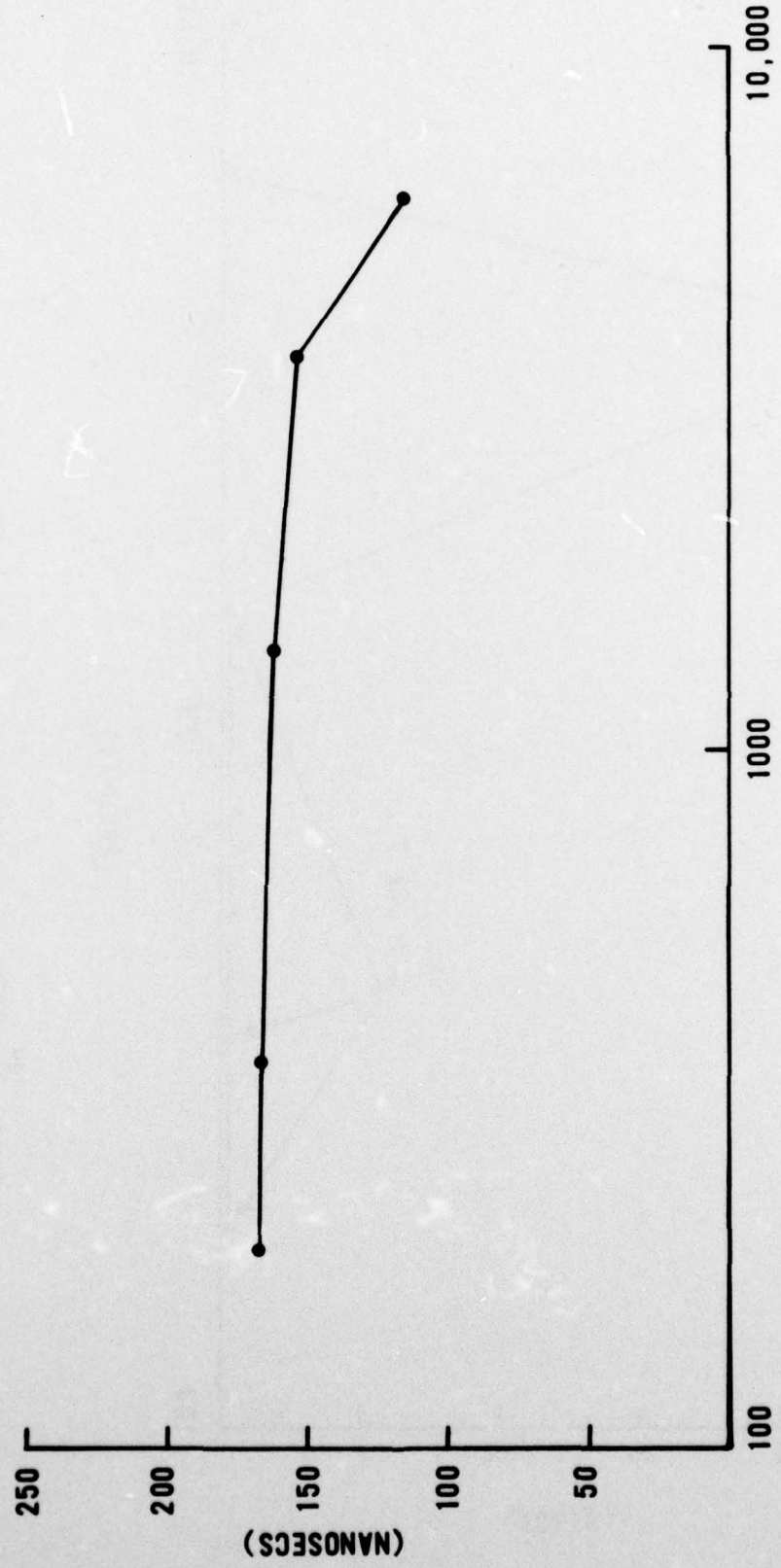


Figure 26. MM74C164 t_{PLH} vs. Total Gamma Dose

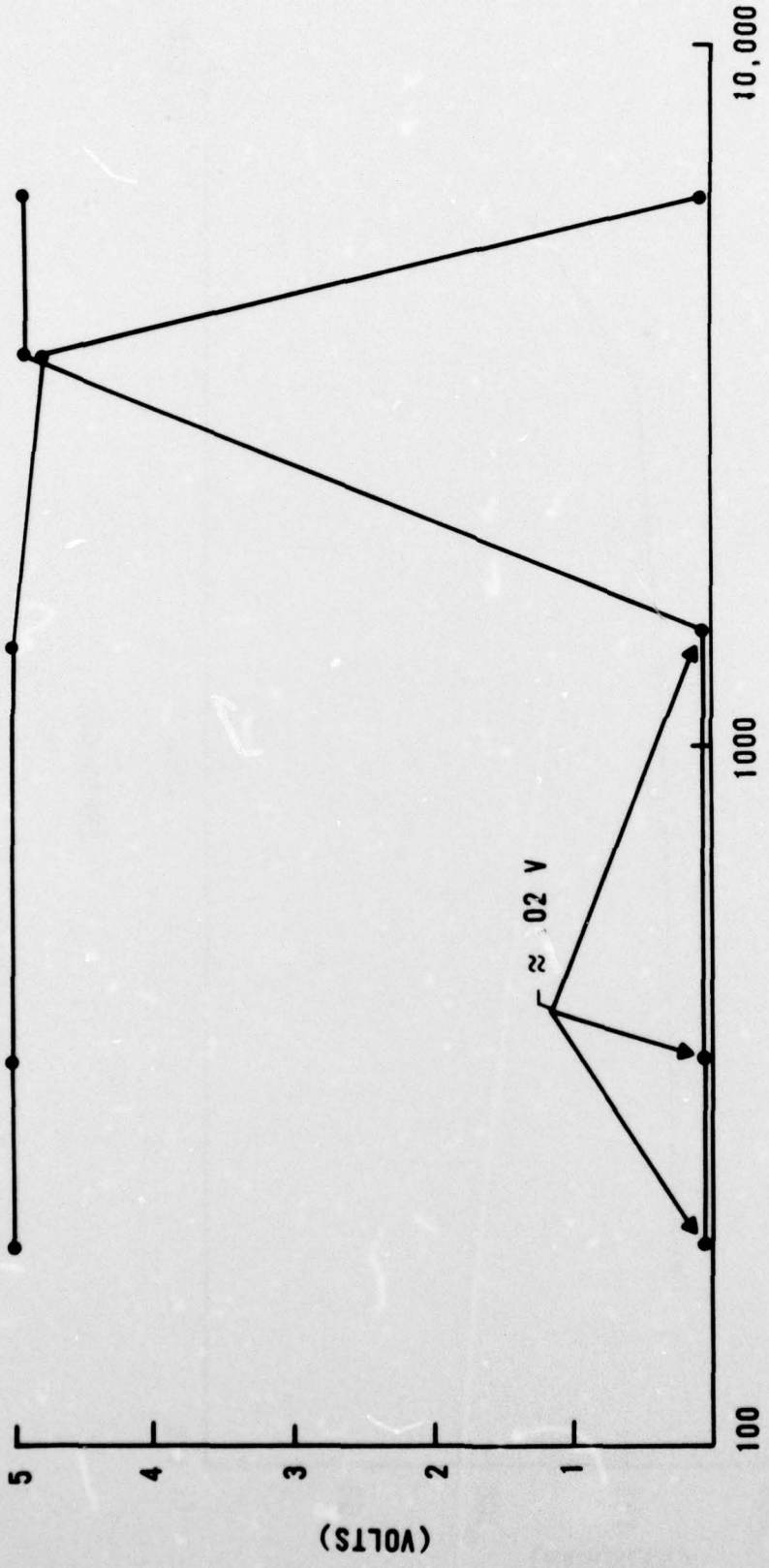


Figure 27. MM74C163 Output Voltage vs. Total Gamma Dose

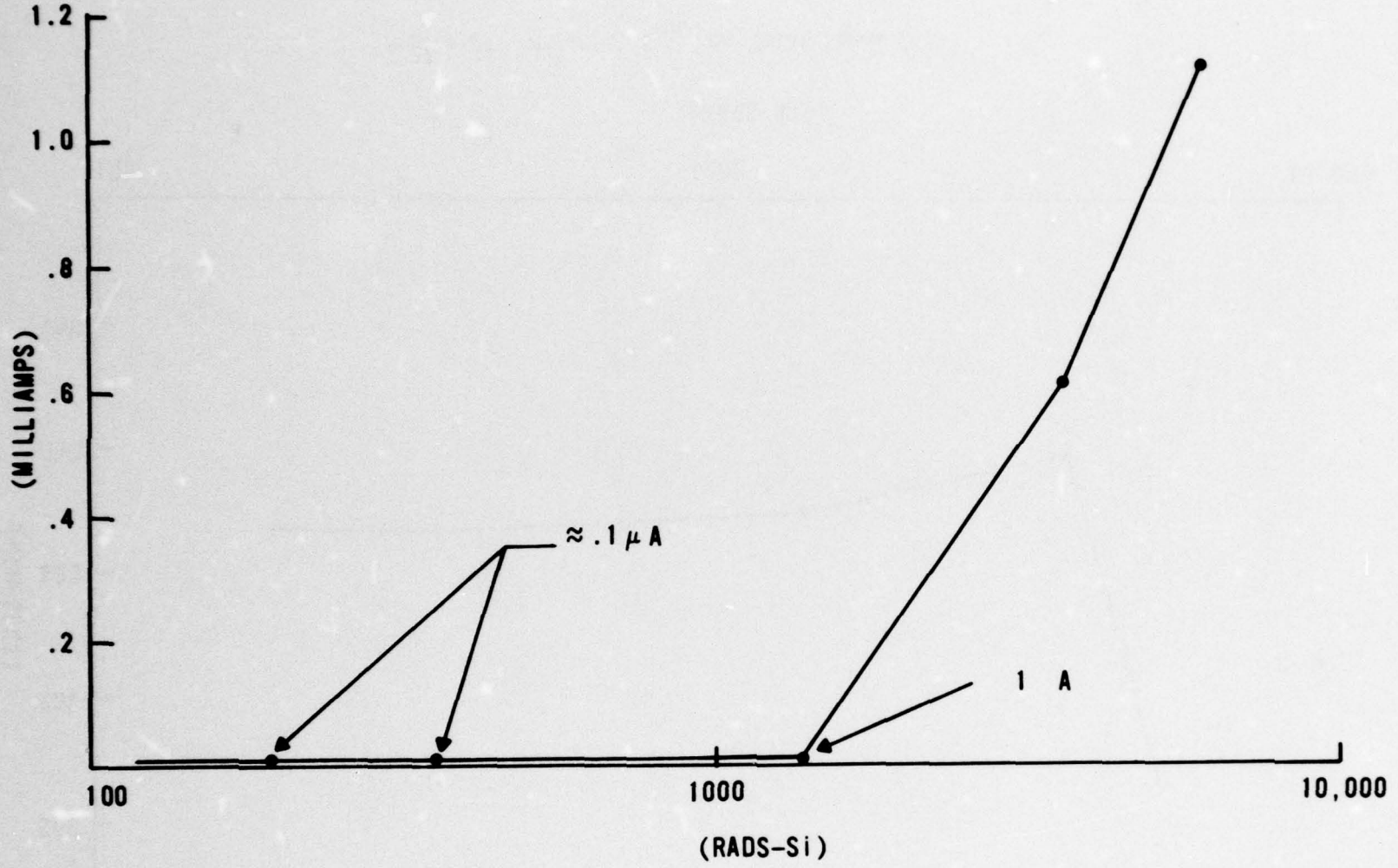


Figure 28. MM74C163 Supply Current vs. Total Gamma Dose

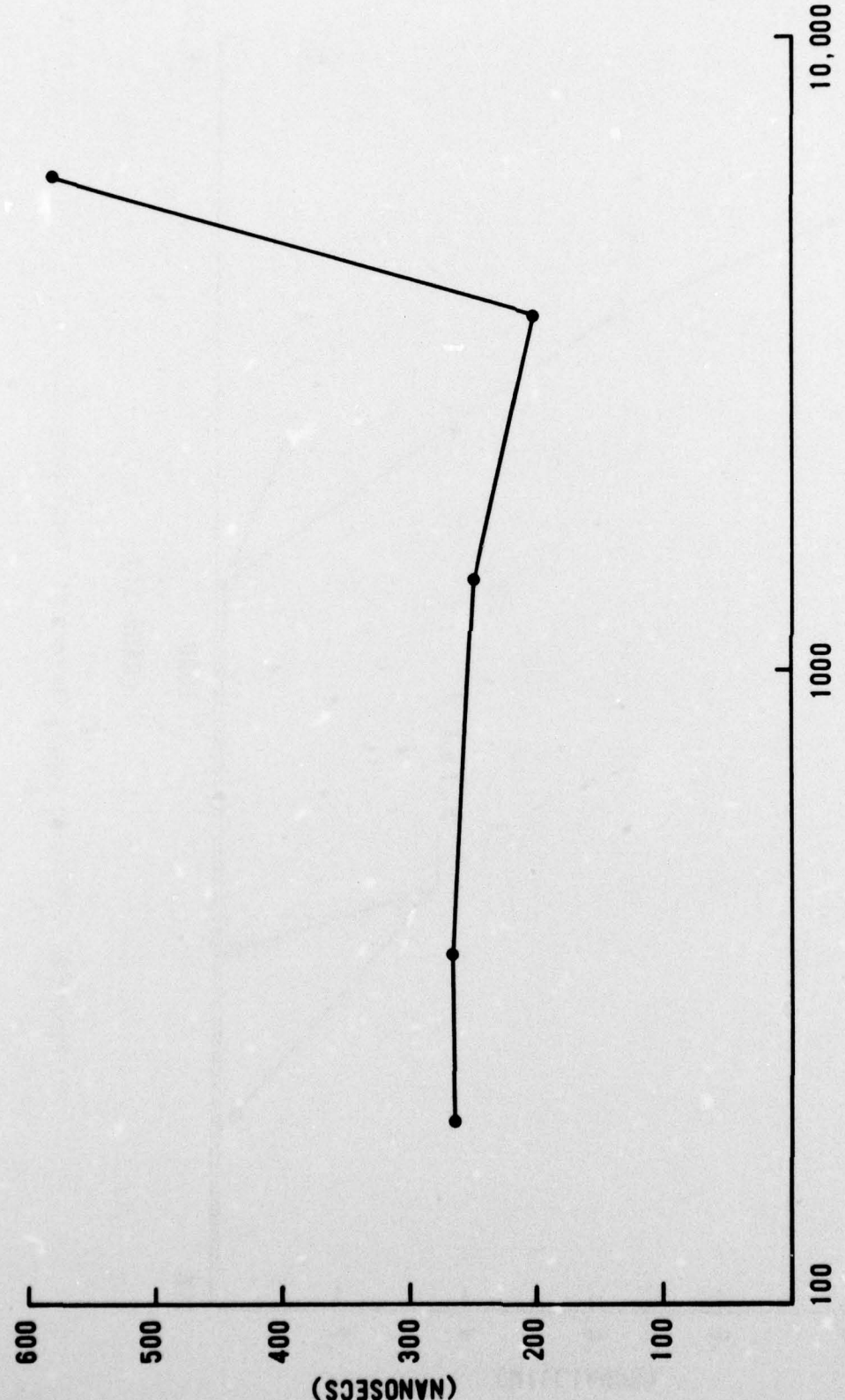


Figure 29. MM74C163 t_{PHL} vs. Total Gamma Dose

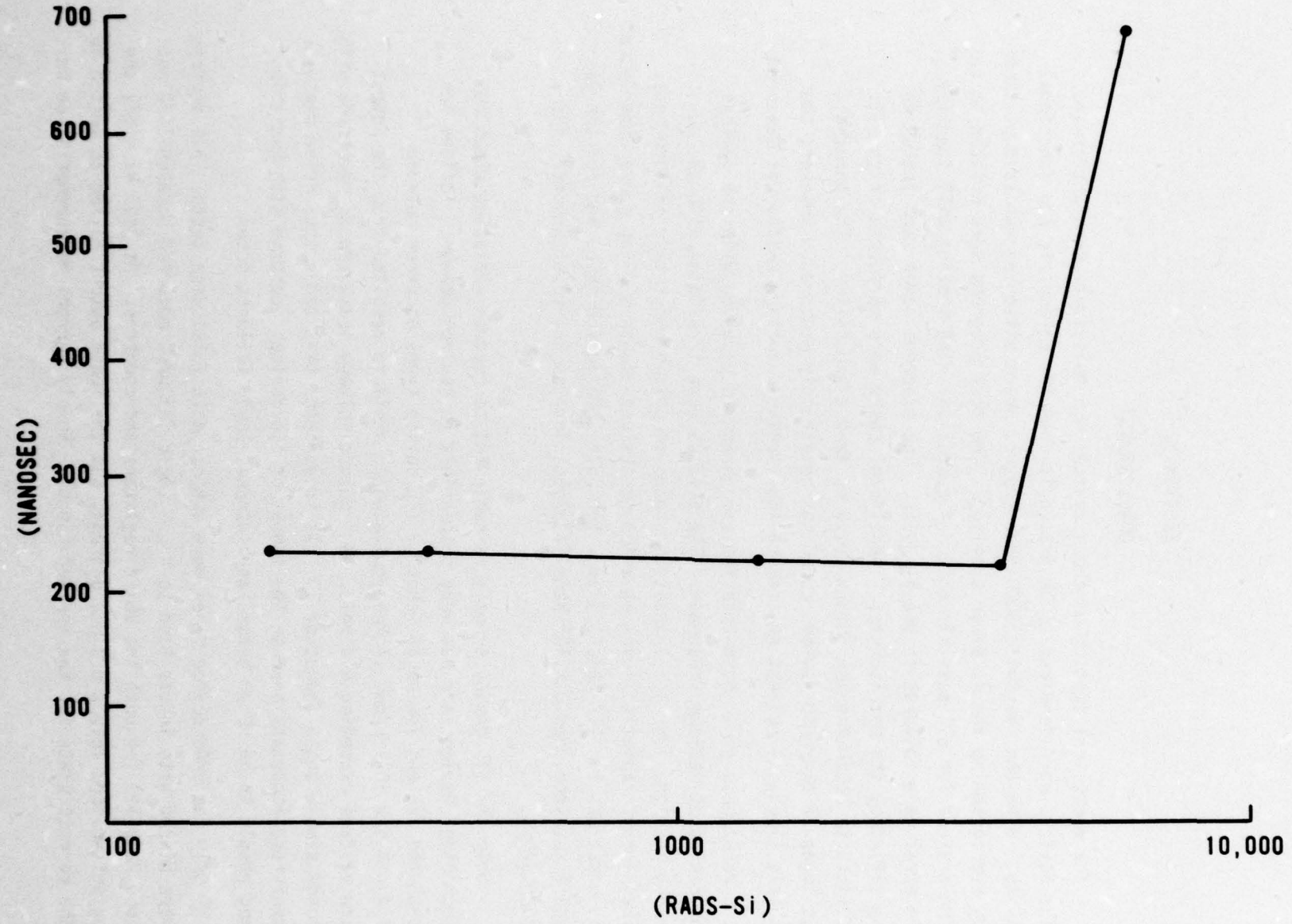


Figure 30. MM74C163 t_{PLH} vs. Total Gamma Dose

SECTION VI

CONCLUSIONS

The electrical testing of these devices was relatively straightforward. The devices were required to be preconditioned for parametric and functional tests. With the Fairchild 5000/5800 tester, preconditioning was accomplished by reprogramming the dc power supplies. The test programs were written to test the devices for all possible modes of operation. The testing will identify internal gate failures in the circuits. The external modes were tested as specified by the manufacturer. Additional tests were performed on the TTL devices to determine the output drive or fanout capability. The threshold voltages of the CMOS devices could not be directly measured. However, the supply (leakage) current related to the threshold voltage shifts was measured.

Worst case gamma dose-rate failure threshold occurred with the devices operating at maximum frequency. The devices were irradiated with the output being in high, low, and transition states to obtain worst case failure mode. The highest radiation level at which no devices within a given group experienced an upset was 2×10^8 Rads(Si)/sec. for both CMOS device types and for the TTL shift register, and 3×10^8 Rads (Si)/sec. for the low power Schottky TTL counter.

Only the TTL device types were subjected to neutron radiation since MOS technology devices are not very susceptible to neutron damage. Failure for both the TTL and low power Schottky TTL device types occurred between $1.4 - 4.6 \times 10^{14}$ n/cm^2 (1 MeV equivalent). Failure resulted from the output low voltage exceeding 0.8 volt. The output voltage measurements were made with loads simulating a fanout of 10. It is apparent that the output drive measurements are important because the fanout of the devices decrease with radiation and result in an error before any internal logic failures occur.

Only the CMOS device types were subjected to total dose tests. All devices were biased with inputs tied to V_{CC}. Logic failures occurred between 1490 and 3656 Rads(Si) for both the shift registers and counters. At 3656 Rads(Si) the output voltage levels did not degrade, but the logic output failed to switch to the correct state for the applied inputs. Supply current measurements can be

used to predict this logic state failure which is caused by n-channel threshold shifts.

In conclusion, the electrical tests performed on these sequential logic circuits enabled excellent radiation characterization of the circuits.

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